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DESIGN OF THE 4 BIT RIPPLE CARRY ADDER USING DOMINO LOGIC AND CLOCK DELAYED DUAL KEEPER DOMINO CIRCUIT

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Abstract

Today in the modern world, the technologies have been developing in designing the CMOS VLSI circuits by optimizing the leakage power, propagation delay in the deep sub-micron technologies. In few decades back power and delay consumption is more in the implementation of the transistor level design. The consumption of area increases similarly it increases its delay and energy efficiency. To overcome these major challenges, the DLC is proposed. The DLC consists of the precise keeper control which significantly increases the action of the operation. The positive feedback circuit is connected by a feedback to keeper circuit excessively to propagate the delay variance to the circuit. Over here standard high-speed clock delayed dual keeper is proposed with the keeper circuit that is made up of two keeper devices. This CDDK impressively bring down the power and thereby the rate of the circuit is elevated. By the CDDK the basic gates are implemented and analyzed the consumption of power and delay variability against the conventional domino logic by Monte-Carlo simulations. Additionally, the Monte-Carlo simulation is for the 4-bit ripple carry adder implementation and the reduction of energy efficiency and delay variability are demonstrated. The result comparison is done in case of the prosaic domino logic circuits. Analysis of the circuits is fulfilled by the cadence virtuoso tool by using 90nm technology.

Keywords: Domino Logic Circuit, Clock Delayed Dual Keeper Circuit, power consumption, Monte-Carlo simulations, 4-bit Ripple Carry Adder

Introduction

In the submicron mode system works towards the low consumption of power and a more speed performance among other type of circuits, a domino circuit has a significant consequence. The speed comparison of the domino is characterized on basics style PMOS as the precharge and pull-in-network and nmos as evaluation transistor in the PIN. The domino circuit has been making an extreme effect in indicating the requirements of speedy and low-power saving devices. The concept of the large fan-in in the operation of the domino logic design is more remarkable contrast to the conventional circuit because the logic design of domino escapes layering of transistors in the network blocks PIN. The circuit perform of DLC is maximum of 2X times faster than compared to the CMOS logic. The leakage current is gradually increases due to numerous paths to ground. The DL circuit initially consists of a pre-charge transistor that is controlled by the clock signal CLK as the input. During the PRIMITIVE stage the clk signal the re-loading voltage transistor operates the D node to charge to HIGH state and this phase of operation is known as the pre-loading phase and then in evaluation phase the CLK signal is represents HIGH state then the pull in network performs during the analysis stage [1].The domino logic circuit is an exact from as that of clocked CMOS circuit. Here the precharge, evaluation phases and clock were used for a cascaded series of domino logic block. A conventional dynamic circuit needs MKeeper transistor to defend the level of the D node in case of splitting of charge, outflow of current and source of noise. In the mainstream domino logic that integrate Mpmos keeper to refresh and to keep the D node HIGH against the intrinsic noise source such as a gradual transfer of current and splitting of charge affects the D node during the FALSE state evaluation of

the PIN . Though if PIN accurate the charge at the D node that carry out to the pull network invariant as the keeper seeks to sustain the D node HIGH [2]. The result of the MKeeper transistor can improve the performance of reliability and speed. The k correspondence is stated as

$$K = \frac{\text{Wkeeper}}{\text{WPIN}}$$

Where Wkeeper is the distance across the keeper device and WPIN distance across the estimation phase transistor in the PIN that resolves the robustness and reliability of the circuit [3].

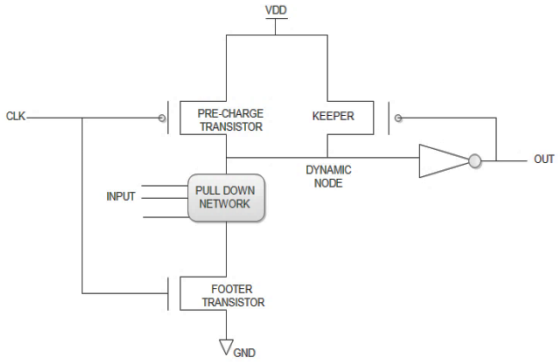


Figure1. Conventional Domino circuit

The compliment loop combines the circuit of the keeper domino circuit additionally provokes the change of the delay and the outcome of the process modifications in the delay of the dynamic and static CMOS are analyzed in the depth as a function of the circuit specifications. The objective of the delay variability depends upon the circuit parameters like number of arranged transistors like fan-in their capacitance of load, size and circuit topology. The variability of the delay is doubled when compared to the static logic consequent the keeper circuit transistor [4]. The growth of low technology nodes executes current leakage, supply and threshold voltage are major occurring factors. The threshold leakage of current is defined as Is1 and the gate oxide leakage current is defined as Ig1 defined major elements of the domino circuit and such component convert domino circuit as a high sensitive circuit, the small input noise that tends to the reduction of robustness and it also been note that the state of the clock and the combinations of input holds an extreme impact on the mechanism of the outcome of the transistor or robustness and even when accuracy of speed is increased. The study seeks solutions related to increases of leakage current, increasing of complexity of the keeper circuit transistor current consequent, extended noise margin and resultant an extreme delay and rise of charge and disparate measurements are obtained. The mutation of the domino circuit improves reliability and momentum of the domino circuit [5]. The domino logic acquires the extreme throughput caused by minimum a noise margin collated to the conventional CMOS. Reduced noise margin indicates a rise of acuteness of the domino logic circuit towards the noise source. In domino logic circuits noise exception can increase by downscaling technology. This scaling factor increases the energy efficiency of the circuit. Hence to decreases consumption of power the voltage supply is scaled down then delay in the circuit increased and satisfies the threshold delay scaling voltage is done through voltage supply scaling. The reduction of threshold voltage boosts up the speed of the domino circuit reduces the immune of noise of the circuit by increasing of the leakage sub-threshold current. The technologies of scaling abate the concentration of the gate oxide that generates a sharp growth of sub threshold, leakage current at the gate and the overflow of current. Due to overcome off current, the noise source and low threshold voltage makes to lower the execution of the domino circuit at extreme frequencies. The scaling of the devices leads to increase the overflowing of the current of the domino circuit by the Small Channel Effects. The small

channel effects reduces efficiency of the length of a channel in the device due to the reduction of the efficiency of the length the threshold voltage also reduces [6].

The average power of the domino is stated as

$$PL = P_{leakage}+P_{short}+P_{switch}$$

The voltage at D node can trickle due to the overflow of current over NMOS transistors in the PIN block. The source of noise of supply that becomes inadequate beyond scaling the technology to control this problem, the keeper transistor is put upon. The major disadvantage observed by using MKeeper transistor, the noise margin leads to confliction along the D node and the Pull down the network. Hence it leads to large power and speed degeneration.

The techniques for the power reduction of the dynamic D gates are proposed

a. The swing of the voltage of D node reduces.
b. The execution of the keeper is improved.
c. The estimation node is modified and restricted.

The approach for the first model is more efficient during the power of dynamic CMOS is proportional to the voltage move back and forth leads to power saving. The advantage of next perspective of the dynamic power leads to the decreases the conflict current by a smart keeper circuit. The next approach of the domino circuit that is proposed was a Modified Charging Based Domino circuit that can stabilize the reducing the large amount of lose power in large fan-in gates [7, 8, 15]. The static output reduces through voltage swing at D nodes are continued keeping the preceding assert charge of the D node during the consecutive precharge and as a result the reduction of energy efficiency is observed [9, 10]. The D node is in the drifting condition during the time of delay and produces the utilization of power and outflow of current reproduction is in the fig.1. Hence the sturdiness of the keeper is be in charge of current mirror circuits reconstruct the outflow of the current in the PDN [11]. This technique is utilized to reduce the robustness and to increases the power dissipation when it is practiced in the fan-in circuits. If the PMOS is in the grounded state then the additional transistor is kept in progress to reduce gain in the loop that is produced. The grounded PMOS is observed in the fig. [12]. The foot-driven stacked transistor domino logic (FDSTDL) the circuit consists of an auxiliary recharge path used to control the obtained output and delay reduced by foot node voltage [8].

The proposed CDDK circuit reduces conflict current describes for increased delay enabled by the keeper that is performed with the auxiliary keeper transistor Mk2. The auxiliary keeper was kept activated by an inverter circuit that was inaugurated after the delay time. The input signal is a CLK that is associated by the device known as footer of the DLC of CDDK. The formal keeper Mk1 restricts at the terminal of the gate of the domino output [13]

Literature survey

Few decades before the speed and area in CMOS technology circuits had essential reduced by describing the new design techniques done by integrated CMOS circuits, the domino logic functioning of every gate is executed twice. The main problem that occurred by this approach is that a complex gate of 32 AOI gate has no static power but extreme capacitance of output and a significant amount of area has wasted. To defeat that problem they stated a new close-packed high- performance circuit design technique was introduced to use with the CMOS technology. The area comparability of static NMOS or Pseudo-NMOS allows a speed augmentation of 1.5 to 2 and performed without resort of some multiphase and static stability are maintained in the circuit [14]. In the CMOS circuit, power predominate the dissipation of power, by reduces

the voltage supply which active to reduce the dissipation of dynamic power. The overcasting of vdd is crucial effect to reduce reliability problems and by reducing the voltage supply alone causes the huge downgrade in the circuit performance, the vdd, threshold voltage vth to scale down by the circuit performance. To maintain critical path the delay the low threshold voltage is to be utilized.

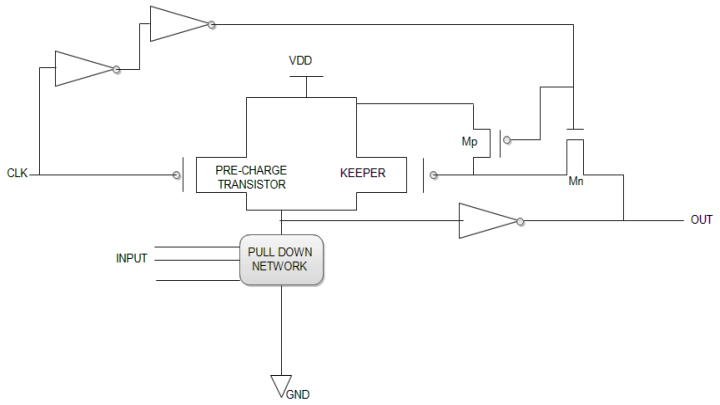


Figure 2. High Speed Domino Circuit

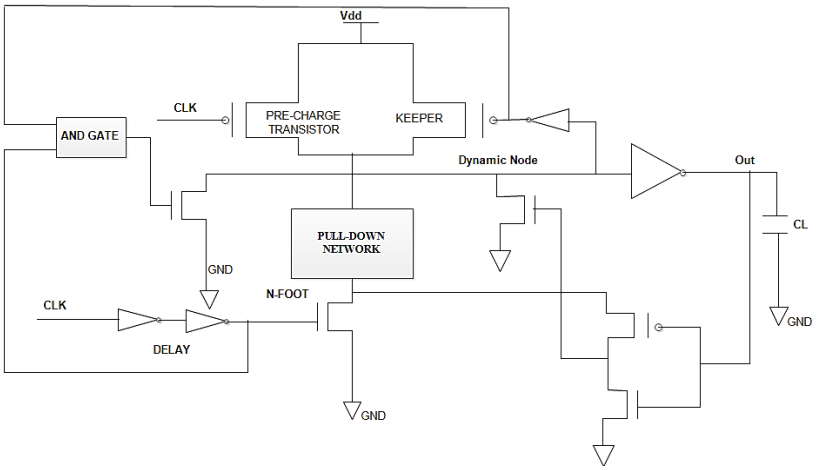


Figure 3. Modified High Speed Clock Delayed Domino Logic

A newly shaped domino circuit was proposed and it is the High Speed Domino Fig.2 Circuit to resolve the drawbacks of the accomplishment and noise immunity in Conventional Domino Circuit. A scaling down approached techniques stated that the speed and the threshold voltage decreased by controlling the noise margin implementing by High Speed Domino, the main objective is that a new modification of the domino logic, circuit is MTCMOS Fig.3 is proposed that momentum and low dynamic power is maintained in the effective mode [15].

By scaling down technology the lower noise margin were becomes more troublesome and the operating prevalence increased by the design of a domino circuit. Here they had proposed a new technique of the domino logic circuit that was common domino logic as evaluation keeper is implemented for the arrangement of the stage of noise integrating, the charge splitting, and the overflow of current. The scheme of perspective was to arrange two keeper transistors where one transistor places as the compact transistor which is used to reduce the current competition and is used to draw the current by the keeper and other transistor is to enhance the noise immunity. The paper stated that the comparisons of different techniques were proposed, but the twin transistor and CMOS techniques are not applicable for all the logic design circuits. The gate discharge delay path length increased in they reproduce technique and the triple

transistor technique. Simple by this survey the main objective that they proposed was the simple feedback keeper is the one that can improve the dynamic logic gate noise immunity towards the entire gates without indicative increases of the area, speed and consumption of power [2]. In this paper they showed a comparison of the different domino logic circuit by implementation of and, or and xor gates the techniques of domino are Footerless Domino Logic (FDL) and by comparing all these they have proposed a techniques named as (FDSTDL) by logic design they had observed a gradual efficiency of power, delay and immunity of noise [6].

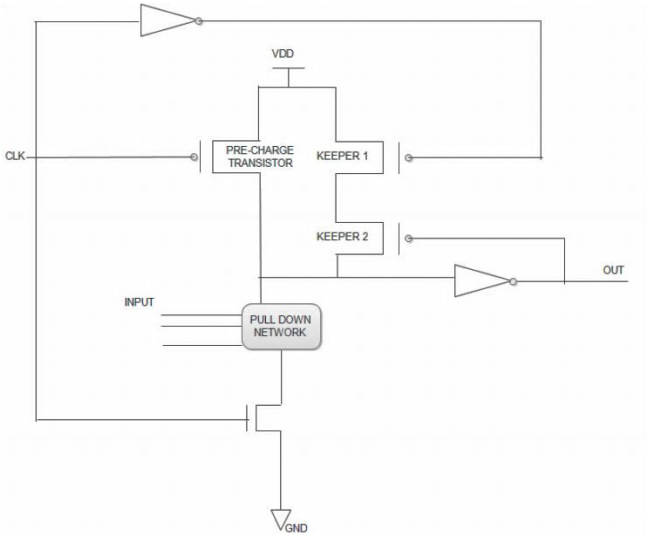


Figure 4. CDDK Domino Circuit

By introducing the CCDK Clock Controlled Dual Keeper the increase of speed performance by reducing off energy efficiency derived and a Novel CCDK technique is proposed that by reducing the contention current that could generate more speed while operation circuit and finally the AND , OR gate implementation of the novel CCDK are proposed[1,2].

The main objective of this survey studies that high delay variability, power and noise immunity are the crucial drawbacks occurred in the dynamic CMOS technology. To overcome such factors the domino logic circuit is introduced and implemented to reduce all the factors like delay variability, consumption of high power and noise immunity. This survey made to overcome these techniques by implementation of the adders design by conventional and the domino circuit technologies.

Domino logic circuit

These techniques are broadly applicable by the extreme performance in microprocessors by increasing momentum and region attributes of the DCMOS circuit compared to SCMOS. This circuit design is a CMOS based evaluation of the dynamic logic techniques which works on the principle of either the PMOS or NMOS transistors. The prosaic domino circuit which consists a PMOS transistor M1 represents at PIN and NMOS transistor is connected along the PIN requirement of the logic at the NMOS footer M3. By this technique the representation of more transistors been gradually decreased from 2N to N+2 which had reduced area and utilization of power.

When the clock signal (CLK) is at the dispirited state the precharge form of the node D to logic HIGH occurs over the PMOS transistor M1. During estimation the stable state the PIN path is disabled and PUN path enabled. When the clock signal (CLK) is the HIGH state, the precharge state discharges and the evaluation

phase starts evaluating then the node D discharges stationed upon the inputs of PIN. The charge outflow at the D node has satisfies by PMOS keeper transistor M2.

The domino logic circuit can run the operation as fast as possible compared to the static CMOS technique. The speed is 1.5-2X times more than that of conventional logic because the dynamic gate represent low input adequacy along the same output current and a low interchanging threshold.

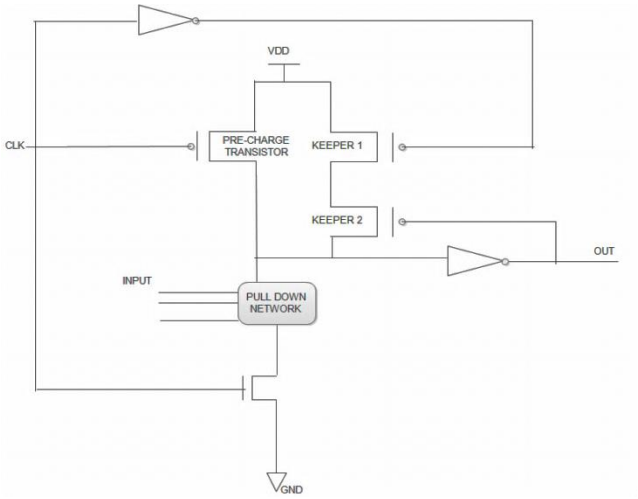


Figure 4. Domino Logic Circuit

Results and Dicussions

The comparison of the power and delay variability is calculated and analyzed below in this proposed technique. The result obtained by the comparison of power and delay calculation of 4 bit ripple carry adder are defined by the cadence virtuoso tool that the power is gradually got down in domino logic when compared to the conventional logic. The graphical representation fig.5 explains the power resulted in XOR gate is high and the remaining is low compared to the other gates. The power calculations of the power are defined in a tabular as:

Table 1 Comparison of Power calculations

S.No.	NAME OF GATE	CONVENTIONAL LOGIC	DOMINO LOGIC
1	AND GATE	22.04E-9	19.4E-9
2	OR GATE	57.6E-9	31.01E-9
3	XOR GATE	114.8E-9	111.4E-9
4	FULL ADDER	368.6E-9	111.1E-9
5	4-BIT RIPPLE CARRY ADDER	716.5E-9	548.5E-9

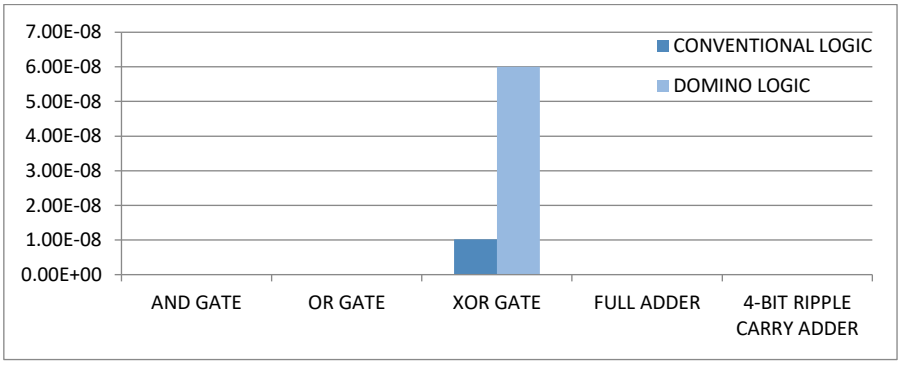


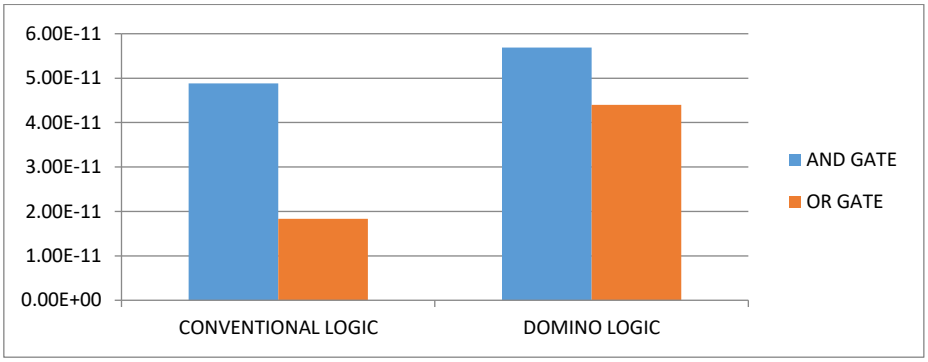
Figure 5. Graphical representation of energy efficiency

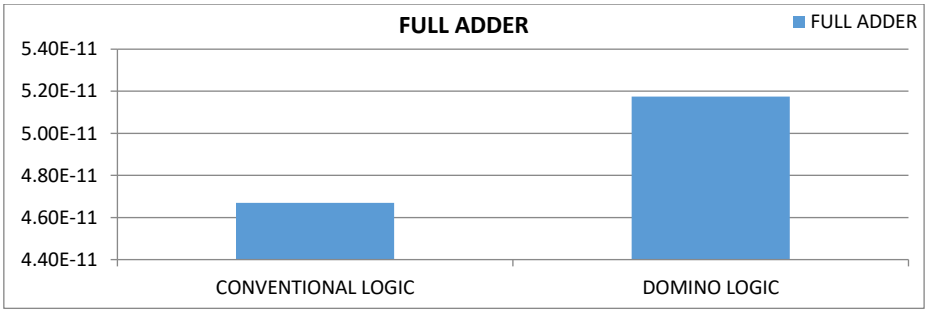
The power obtained for the conventional domino logic 4-bit ripple carry adder is 716.5E-9 is gradually reduced to 548.5E-9. The main drawback of the proposed technique is the delay in the circuit is increased delayed values c form as:

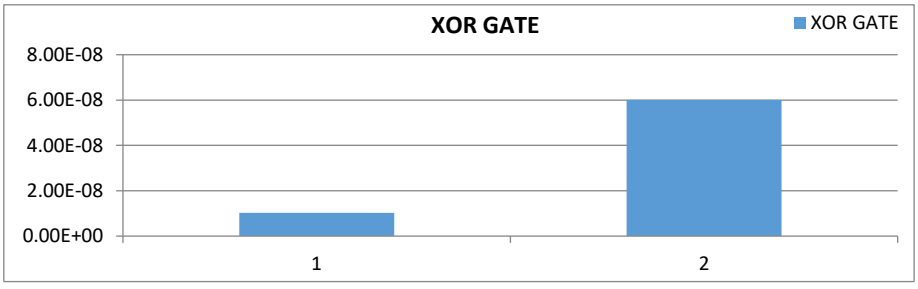
Table 2. Comparison of delay calculations

S.No.	*NAME OF GATE*	*CONVENTIONAL LOGIC*	*DOMINO LOGIC*
1	AND GATE	48.8E-12	56.9E-12
2	OR GATE	18.3E-12	44.0E-12
3	XOR GATE	10.18E-9	60.05E-9
4	FULL ADDER	46.69E-12	51.75E-12
5	4-BIT RIPPLE CARRY ADDER	85.2E-12	93.4E-12

The delay calculations are represented in graphical form fig.6. The delay for 4-bit ripple carry adder is 85.2E-12 in conventional and in domino logic is defined as 93.4E-12. The delay is raised gradually comparing to the conventional in domino logic. The main drawback of the domino logic is that the delay increased gradually between the conventional and domino logic circuits.







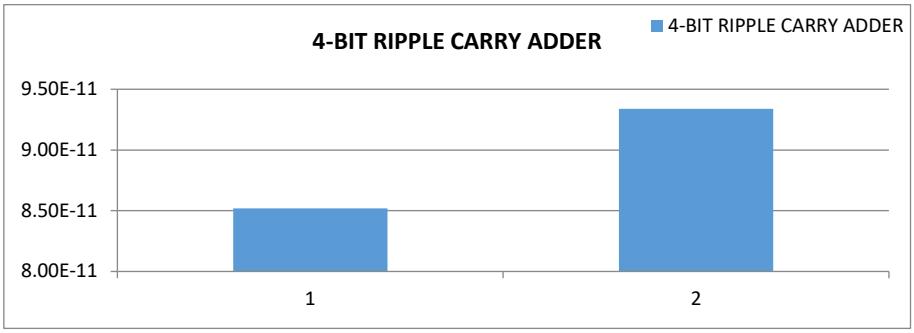


Figure.6 Graphical representation of delay

Conclusion

This survey proposed the difference between the dynamic and static CMOS circuit. The comparisons of the Dynamic and Static CMOS made by the latest technique proposed domino logic circuits and also defined many types in domino circuits. Basic gates are implemented using the domino circuit, the reduction of power, delay variability and noise immunity and area calculations are verified. In this survey the delay is directly depended on the threshold voltage specified at voltage that is observed in this study. Finally, this Domino logic circuit is compared by implementing the ripple carry adder with the conventional and domino logic circuit for the optimization of the area, power, noise immunity and delay in the CMOS VLSI technologies uses in the microprocessors.

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