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A Review on RAM Cell Structures in QCA

[1] Amanpreet Sandhu, [2] Parminder Singh, [3] Archana Goel

[1] *Chitkara University Institute of Engineering and Technology, Chitkara University, Punjab, India.*
[2] *Department of Chemical Engineering, Thapar Institute of Engineering and Technology, Patiala, Punjab, India*.
[3] Chitkara *Business School, Chitkara University, Punjab, India.*

Abstract

CMOS circuit designs are scaling down from 6nm to 7nm in area but one cannot continue to follow Moore's Law because the transistor size is now reaching to its physical limits. New techniques like Quantum-Dot-Cellular-Automata which uses the position of electrons confined with-in a QCA cell to represent the logic state of a memory cell is being utilized. The two types of Quantum based memories are Parallel memory and serial RAM memory. These QCA memories are based upon memory-in-motion paradigm that is memory logic should keep in motion by using QCA cells. Parallel memory architecture design in QCA offers low latency at the cost of reduced density. Parallel memory utilizes one-bit per memory cell like the traditional CMOS Random Access Memory (RAM) design, but in QCA such memory design offers repetition of the Write-Read circuitry for each RAM-cell or a memory bit. It increases the hardware in terms of number of QCA cells, clocking zones and control cells. This structure offers fast operations at the cost of reduced density.

Keywords: Quantum Dot Cellular Automata, Serial Memory, Parallel Memory, RAM Cell.

1. Introduction

From the past five decades, the conventional Complementary Metal Oxide Semiconductor (CMOS) paradigm follows Moore's Law, where the number of devices on a single chip double in every 18 months Joachim, C., J. (2000). This trend results in decreased feature size and power dissipation with higher device densities. But due to the scaling down of CMOS to submicron, many limitations occur. The challenges like un-deterministic leakage currents, quantum tunneling and short channel effects hinder the further scaling down process of CMOS circuits. Hence the performance of CMOS devices deteriorates due to their rapid scaling down to nanometer range. Gordon Moore had mentioned in his article in that the scaling down of feature size can never be a continuous process. The scaling down of a transistor channel length result in leakage currents due to quantum mechanical tunneling. Hence the performance of CMOS circuits degrades at such smaller scales.

2. Quantum Dot Cellular Automata`

Many authors have tried to define Knowledge Management showing their perspectives. Some of these are discussed below. QCA is the novel nano-technology that was introduced in 1993. In QCA, the binary levels are not depicted as +V or –V volts but they are saved as the placement of individual electron in a QCA cell. Bistable charge configuration is used in QCA to represent the binary states. A QCA cell contains four quantum dots that are placed at an extreme corner of a QCA cell. The charge in it is placed in the form of a quantum dot. It is made up of compound semiconductor material gallium arsenide.

3. Fundamentals Logics in QCA

A cell is the fundamental element in Quantum dot Cellular Automata Tougaw P. D. et al. (1994). Each cell is representing a binary logic by an appropriate configuration of electron charge. It contains four quantum-dots. Each quantum dot is made up of a semiconductor nano-material that shows quantum-mechanical effects. The two out of the 4 dots occupying electrons in a “diametrically opposite” locations. These electrons are placed at the opposite corner (diagonal) of a QCA cell because the Coulomb repulsion in a diagonal position is less as compared to an adjacent position. The coupling of quantum dots is done by tunnel junctions.

3.1 QCA Wire (90 degree)

The cells can be placed in adjacent to each other to form a wire. The electrostatic force between the cells helps the electrons to occupy their positions within the cell. The position of an electron within a QCA cell depicts the logic state. This logic level can be moved to the output QCA cell along with a QCA wire is due to the polarization between the adjacent cells. Lent CS et al. (1997)

3.2 Logic Gates in QCA

The three logic gates in QCA ate Majority gate, AND gate and OR gate. In the majority gate, the majority of the inputs wins at the output, for example if ‘100’ is applied to inputs, the output obtained is ‘0’ which represents the majority of inputs. In proceeding sections, the literature review on the origins and development of QCA and literature review of memory cell Structures are presented.

4. Literature based on Origin and Development of QCA

The literature related to the origins and development of QCA and RAM cell structures using QCA is described in this section. Lent C S. et al. (1997) presented QCA based quantum devices which work on the nonlinear columbic interactions for performing various useful computations. The idea is based on a QCA cell having two electrons placed in their respective quantum dots. When these cells got fully polarized, they achieve two states. One is positive polarization and the other is negative polarization. The density of polarization is very high. These new structures can easily be fabricated for performing important computations at the circuit level. Hence, they were able to build QCA device arrays for computing at nano scale level. Tougaw PD et al. (1994) in 1994 studied the possible implementation of basic logic operations (AND, OR) with new primitive gate named as majority gate using QCA cells were examined. The conclusion part shows the coupled quantum dot cells can be utilized for implementation of three basic Boolean logic gates i.e., AND, OR, and NOT gate. In addition, other new QCA implementation such as-as majority voter has also been introduced. In addition, the structure of the binary wire is formed by using linear arrays of QCA cells. Various coplanar wire crossings have been implemented using QCA. In order to verify the efficacy of proposed primitives, an exclusive OR gate has been formed. By using the mentioned structures more complex design a full adder has been demonstrated. These structures prove the working of basic logical gates based on QCA. Joachim C et al. (2000) examined the NOT gate and how the binary wires have been implemented with a series of QCA cells. The integration of various electronic components has been done using mono molecular electronics. Here the logic Progression of elements like QCA based wires,

switch, and various amplifiers have been assembled using a single molecule assembly. Lent CS et al. (1997) presented the working of QCA circuits according to the truth tables a new adiabatic clocking scheme has developed which further increase the speed of circuits at the nano level. The invention of adiabatic switching enabled the QCA circuits to perform the complex computations in a fraction of seconds. The clock-controlled circuits eliminate meta-stability and improve step by step functionality. Porod W et al. (1997) showed the possible implementations of QCA structures have described. The author proposed a new paradigm of coupling the quantum dots. Here a combination of various QCA cells performs various Boolean functions to form nonlinear networks. These networks can also perform various analog functions at such a nano scale paradigm which is based on cells having couples quantum dots. The logic functions for nonlinear networks can only be implemented on specific cell arrays. Snider GL et al. (1998) experimentally demonstrated the transistor-less paradigm with a basic cell of QCA. This nano technology offers many advantages over FET based technology because of its small size and efficiency to work with quantum effects. The interactions form logic states of QCA circuits. For example, positive polarization represents logic state 1 and negative cell polarization represents logic state 0. Here the signal is encoded as voltage levels. As the electrons are confined in a QCA cell, there is an absence of flow of current i.e., only charge or polarization state travels in the circuit. It makes computing much more efficient at the molecular level. The dots are fabricated from aluminium islands and tunnel junctions are formed by aluminium oxide. Orlov AO et al. (1999) the experimental demonstration of QCA cells as a binary wire has presented. QCA as one of the important paradigms performs various experimental computations to construct a binary wire. The binary wire contains a group of QCA cells having two quantum dots and a single electron. These QCA cells are capacitive coupled with each other. The input signal applied to the first QCA cell of a binary wire makes it fully polarized. Any QCA cell placed adjacent to this polarized cell will also achieve the same polarization state. Hence the columbic charge of one QCA cell interact with its adjacent cell to make the line of cells fully polarized with the same state. The electrometers are used to measure the polarization of a cell. Bernstein GH et al. (1999) observed the switching speed of a QCA cell is experimentally demonstrated. A number of experiments have performed on metal junction or tunnel junction-based systems to investigate the switching states and properties of QCA cells. During the experiment, it has been observed that as the electrons tunnel of the dots in a cell induces an opposite switching in an adjacent quantum dot. Ongoing experiments determine the cell properties having all the four quantum dots possesses tunnel junction coupling. This results in much higher polarization at the output. Niemier MT et al. (2000) developed a QCA simulation tool in 2000 on which a CPU is deigned and simulated. Here the two quantum dots were made to place 10nm apart with the dot diameter of 10nm. The center-to-center distance between the two QCA cells was taken as 42nm. Niemier MT et al. (2001) describes a set of rules to implement a simple processor using QCA is developed. Various solutions to the problems occurred during the floor planning has been solved. Timler J et al. (2002) calculated the power dissipation in QCA. They have shown that the clock restores the energy lost during the dissipative process, and molecular device densities achieve the ultra-low levels of power dissipation. To measure the power dissipation in QCA based circuits, a density matrix-based approach has developed. A QCA cell has described using a two-state model for the quasi-adiabatic switching scheme. Further, it has been proved that the power loss in a QCA circuit is restored in a clock. Smith CG et al. (2003) presented QCA devices were fabricated on gallium arsenide aluminium gallium arsenide doped hetero structures by considering electron beam lithography process. Here the four dots system polarization has tuned to 1 two-dot

polarization. Haider MB et al. (2009) conducted the experiments that a quantum dot can be created using silicon atoms dangling bonds. The switching time of the cell is of the order of a microsecond. Pierre M et al. (2011) presented various quantum dots by using standard MOSFET technology at 4.2 K temperature. These silicon dots are fabricated for silicon nanowire. Sangghaleh F et al. (2013) measured the existence of one silicon dot for a lifetime. It has created by means of the lithography process and ion implementation. They observed that there is a large dot to dot variance in photo luminance decay for the time span of 5 to 45 micro seconds. Huang J et al. (2007) A new technique 'processing-by-wire' is proposed for designing QCA based tiles. Simulations for various kinds of cell defects have been characterized. The results show the fault tolerance behaviour of the design. Khan A et al. (2017) presented two types of sequential designs, Hazardous and Non-hazardous design. Both designs have been compared for kink energies and proved that the hazard-free designs are much more efficient. Spruijtenburg. P. C et al. (2018) has described the importance of material property and fabrication process for creating the silicon quantum dots. The important processes such as oxidation, layer deposition and vapor depositions need to be tailored to prevent various defects and disordering of the system. Maslova NS et al. (2019) the effect of tunnelling on resonant oscillators has been analysed in a noisy environment. The results prove that the switching rate of QCA cells has strongly depended on the tunnelling rate. The cells will achieve a stable state at high amplitudes of tunnelling energy.

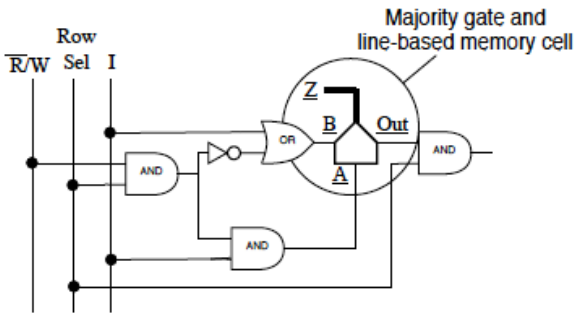
5. Literature based on RAM Cell Structures

CMOS circuit designs are scaling down from 6 nm to 7nm in the area but one cannot continue to follow Moore's Law because the transistor size is now reaching to its physical limits. New techniques like QCA which utilizes the position of electrons confined within a cell to present the binary state of a memory cell is being utilized Taskin B et al. (2009). The two types of Quantum based memories are line-based and loop-based design. These QCA memories are based upon memory-in-motion paradigm i.e., memory logic should keep in motion by using QCA cells.

5.1 Line Based RAM Cell

In line-based architecture, the bits are stored in a straight line of QCA cells by moving the bits in the back-forth direction as shown in Fig. 1. The three columns shown in Fig. 1 represents three clocking zones. In QCA designer software by default four clocking zones is available. By utilizing these four clocking zones efficient memory-cell design can be achieved. Fig. 1 shows the line-based RAM structure.

Figure 1. Line-based RAM Structure [Berzon D et al.]

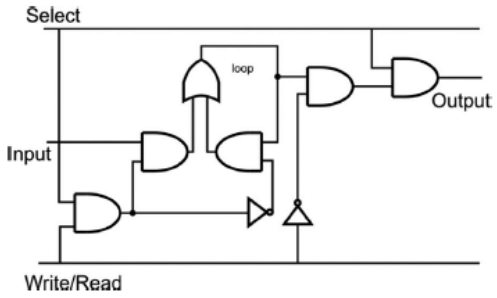


In this section, a literature survey based on line-based approach is described. Taskin B. et al. [19] (2008) presented a line-based approach having double phase clock architecture. The proposed structure out performs in terms of complexity, latency and throughput. For physical verification of proposed RAM cell, QCA Designer software has been utilized. The interaction of the RAM cell with a simple AND gate structure has been introduced and in Vetteth A et al. (2009) presented a shift register is used for designing a memory structure. The main advantage of line-based architecture is its denser performance and précised clocking zones alignments. The dual-phase design has linear Read/Write latency in terms of a number of bits stored in each row. Hence the presented design has two times improvement than triple-phase line-based memory architectures. The Read/Write time of the design is constant as compared to tile-based design. The proposed design requires an external circuit to store the bit after a read operation. In addition, the tile-based memory also requires additional circuit like counter for its Read/Write operations. Hence both types of memory structures require additional circuit for the complete operation.

5.2 Loop-Based RAM Cell

A loop-based design utilizes memory-in-motion paradigm within a QCA loop. In this section, a literature survey based on a loop-based approach is described. Figure 2 shows a loop-based RAM structure.

Figure 2 Loop Based RAM Cell Structure [Walus K et al.]



Berzon et al. (1999) presented a shift register-based memory cell. Here, the bits are required to be shifted between the cells which are an inherent capability of a QCA system. Here an extendable QCA wire is used to carry the data bit for every four SQUARES. The presented memory is loop-based where the number of SQUARES present in a loop has been used to shift the data bit. Vetteth A. et al. (2003) in this paper, authors explain the QCA nanotechnology and its advantages over conventional CMOS technology. Then they have designed various types of flip flops structures using QCA technology. Then the comparison of proposed QCA based designs with the traditional CMOS based on the occupational area has been done. From the results, they have concluded that the proposed QCA based designs have an extremely small size than the conventional CMOS based designs. All the measurements were taken based on QCA cell. The flip flop layouts were designed using QCA on a single layer. Hence the complexity of multilayer structure and cross overs in CMOS has been eliminated in proposed structures. The clocking schemes have been applied very carefully so that the data bit displayed at the output should possess minimum delay as the rules to implement the clocking scheme in QCA structures were yet to be discovered. The reduction in device dimension is also due to the presence of majority gates. Walus K. et al. (2003) Here the author has

designed a new QCA based RAM cell structure. The memory cell is loop-based i.e., the storing mechanism is achieved by constantly circulating the data bit around the loop. The memory structure has designed using a traditional two-dimensional grid of RAM cells. These RAM cells placed in a row are addressed by a decoder circuit. The mathematical model used for simulating the memory structure is Hartree-Fock approximation. The number of QCA cells consumed by a memory grid is 158. The cell-to-cell center distance of 10nm with a capacity of 1.6 Gbit/cm2. By implementing proper area optimizing technique, the greater density of structure can further be achieved. In future perspective, the design can be made fault-tolerant by reducing the wire crossing structures and possibly applying fault-tolerant algorithms. The design can further be optimized in terms of its occupational area. The proposed Memory structure has the potential to implement in THz range in molecular QCA. However, an important design parameter such as speed is difficult to measure. Huang J.et al. (2007) Detailed analysis of various flip-flops and other sequential circuits has been done. Firstly, QCA implementation of an RS flip flop has been proposed. The structure has overcome the clocking issues which is due to adiabatic switching technology in QCA. Then a new D type, flip flop has designed having exclusive clock timings. Hence, the timing requirement of both the flip flops has been explored by using appropriate algorithms so as to achieve minimum delay. New algorithms have been proposed to achieve proper timing and synchronization in the circuit. The proposed algorithms are efficient enough to divide the structure into minimum clocking zones. The proposed algorithm has a particular sorting mechanism to achieve minimum delay by connecting all the paths using QCA wires. A coplanar crossing has also been the part of a design. The wire gates inserted in the circuit using proposed algorithm need not be optimal which might result in longer delays. Moreover, the proposed algorithm has designed for logical level rather than considering the physical layout of the design. Hence the resulting graph might not be that much accurate. Hence the algorithm requires further improvements. Vankamamidi V. et al. (2008) in this work, a QCA based serial memory design has been proposed. The memory structure is designed using QCA tiles, also referred to as the building blocks for storage of data bits. These building blocks have also utilized for designing input/output circuitry in the memory. The proposed memory structure has followed the memory-in-motion paradigm by following a loop-based architecture with proper timing and control of the clock signal. The proposed design is divided into three zones so that the data bits can move across the concatenated tiles. The storage mechanism of the design is loop-based where the length of the QCA wire is not dependent on the word size. The detailed specification of QCA based decoder design as well as input/output circuitry has also discussed. The comparison of proposed memory with the previous designed has done based on latency, clock timings, cell counts, gate count and various other hardware related requirements. From the comparison results, it has been proved that the memory design presented in this work has a very good figure of merit as compared to other designs in the literature. Shamsabadi A.S. et al. (2009) In this work two types of QCA based D flip flops have been designed by utilizing the inherent features of QCA. It is important to mention that the designed flip flops have the same performance when compared with the CMOS. The proposed Flip flops have designed by proper utilization of timing and control of clock signals rather than just replacing the CMOS logic gates with the majority gates. The proposed designs utilized less cell count, lower latency with the lower occupational area in comparison to the other existing designs in the literature. Many limitations in CMOS technology due to a decrease in feature size leads to its replacement with QCA technology. During the QCA designing, it is important to use its inherent capabilities rather than just replacing the logic gates of CMOS with Majority Gates. The main feature of QCA design is its capability

to control the timing of the data flow. Yang X. et al. (2010) presented the designs of D flip flops which are is auspicious for the future nano design structures with much lower energy dissipation and may improve in terms of clock delays with higher speed of operations. The design is utilizing 03 inverters, 04 gates and a single wire crossover. Dehkordi M.A. et al. (2011) Memory is one of the main parameters used in today's digital structures. To optimize a memory cell in terms of its wasted area, longest QCA line, latency, number of clocking zones, becomes very important. This results in improved QCA memory design having lower energy dissipation, lower complexity and lower latency. In this paper, the two types of RAM cell structures have been proposed using this nano technology. The proposed designs utilized proper clocking schemes with majority gate structures. The tool used for simulating the designs is QCA Designer. The presented structures outperform the designs in literature in terms of occupational area and latency. Hashemi S. et al. (2012) In this work, a 2:1 multiplexer-based edge and level triggered D FF and a RAM cell has been proposed. The presented structures are area efficient with lower latency and number of QCA cells. The simulations engines used were i.e., coherence vector and bistable engines were used for a generation the results. The proposed structures outperform all the existing 2:1 mux-based D flip flops and RAM cell designs in QCA.

Kianpour M. et al. (2012) in this work QCA based16 bits RAM architecture has been implemented. The design is utilizing 16 bits array construct a memory. The design possesses a total delay of eleven clock cycles. Chougule P.P. et al. (2017) presented the design which is realized for processing in-memory (PIM) architecture. In PIM based design, all the calculations and storing of data has done in a single unit. In this paper, the case study of 2-input universal gates has been implemented for designing QCA based flip flops. The proposed design is further implemented as a basic cell for designing PIM architecture. From the simulation results, it has proved that the design dissipates minimum power. The basic cell has an area of 0.04 μm2. The newly designed structures have various benefits over the tradition RAM cell like less feature size, lesser power dissipation and lower latency. The proposed designs have higher polarization. Asfestani M. N. et al. (2017) proposed a RAM cell structure having on two 2:1 multiplexer. The proposed design has set and reset capability. The circuit is designed using a single layer approach without any coplanar cross overs. The simulations of proposed designs have carried out on QCA Designer tool. In addition to the structural analysis, the design is also simulated for power dissipation analysis using QCA Pro tool. The presented circuit is area efficient, lower complexity, fewer gate counts and lower power dissipation. Chakarabarty R. et al. (2018) developed an equation based on SR flip flop that can further be used to design other QCA flip flops like JK, D and T. By using this approach for designing the flip flops, the hardware requirement gets significantly reduced. From the stability analysis, the kink energy plot has been generated for the output cell. The proposed layout uses QCA Designer software for simulations. The newly designed flip flops can be used to construct various memory storage structure in QCA. Hence there is a possibility of designing various sequential designs such as counters and shift registers. Liolis O. et al. (2018) presented a cross bar structure for designing a RAM cell. The methodology helps the designer to construct a memory of any size. The proposed circuit has area efficiency with lower input to output delay.

Sasamal T. N. et al. (2018) presented a 5-input majority gate-based D-FF and RAM cell. The designs were simulated by QCA Designer tool. From the simulation output it has seen that the proposed designs are much more potent than existing structures. The newly design RAM cell has an occupational area of

0.12µm2 with a latency of 1.5 clock cycles. In addition, all the newly designed D flip flops are area efficient. Hence from the results, the level-triggered flip flop uses 14% less area, edge-triggered flip flop uses 33% less area and dual edge-triggered D flip-flop utilizes 21% less area and a delay of 40%, 27%, and 25% less in comparison to other designs in the literature. The proposed structure was designed using single layer without using wire crossing. Zoka S. et al. (2018) introduced an area-efficient D-type flip flop. The design has an important pin named as RESET pin. The presented flip flop has the capability of designing complex memory structures. Rezaei A. et al. (2018) Using an efficient QCA D flip-flop (DFF) architecture, a 5-bit counter, a novel single edge generator (SEG) and a divide-by-2 counter are implemented. Also, some types of oscillators, a new edge-triggered K-pulse generator (KPG) and a negative pulse generator (NPG) are presented for implementation in QCA. The robust layouts of proposed circuits are developed and implemented using QCA Designer tool without any wire crossing. The fault like missing cells and their defects at the output of newly designed DFF were analyzed. Also, the robustness of the proposed QCA designs with respect to temperature variations is examined.

Sasamal T. N. et al. (2019) presented a new rotated 3-input MG. This new gate is designed for single-layer architecture. One can develop complex circuits by using the proposed gate. Here, a novel D flip flop and RAM cell have proposed based on newly designed MG. The proposed designs occupy the less occupational area and less delay. They are coplanar in nature without any coplanar wire cross over. All the simulations were carried out using QCA Designer software. When compared with existing structures, the proposed designs utilize enhanced layout schemes with high performance. Due to the presence of rotated cells, the proposed designs possess a high fabrication cost. Fam S.R. et al. (2019) presented a 2D structure of a memory design using a D type latch. For one bit of read and write data, a single bit RAM cell has been designed. The newly designed structures have less complexity, less occupational area and lesser number of QCA cells. The main drawback of the proposed design is that it is not optimized for latency. The simulations were carried out using both coherence vector and bistable engines in a QCA Designer tool. The power dissipation of the proposed designs was dine using a QCAPro tool. From the results, the proposed designs were much more energy-efficient than the other existing designs in the literature. Binaei R. et al. (2019) presented a flip flop which can further be utilized for designing complex digital circuits. The Flip Flop has an additional feature of set and reset capability. The other complex circuits which can be designed are processors, shift registers etc. These complex designs will take advantage of set/reset feature of the proposed flip flop. In this paper, both the modes i.e., synchronous and asynchronous mode were analyzed for designing a RAM cell structure. Table 1 presents a comparison of line based and loop-based memory cell design. Angizi S. et al. [41] (2015) presents a new 5-input MG design which is coplanar and can be utilized for designing various single layer QCA structures. To measure the effectiveness of newly designed gate, a new RAM cell has been designed which performs better in terms of occupational area, latency. The proposed RAM has set/reset capability with minimum input to output delay and requires less hardware. The proposed design is coplanar.

Khosroshahy M.B. et al. (2017) presents a new 5-input majority gate having high energy efficiency in QCA. The gate can be used for designing single-layer structures which results in the lower occupational area and low complexity. The proposed design can be extended well for connecting other digital circuits. Hence it has better physical connectivity i.e., the proposed gate can efficiently be connected physically for

designing other digital circuits. The proposed gate has further used to design a RAM cell structure. The new designs have simple architecture, less complexity with high energy efficiency.

Moghimizadeh Tet al. (2019) presented two new designs of majority voters which are very less susceptible to fault majority gates. One is 3-input and the other is 5-input fault-tolerant majority gate. Both the gates were assessed for various important defects. The proposed designs were 88.89% and 61.9% less susceptible to a fault. The proposed RAM cell which is much less susceptible to fault can be used to construct memory designs and other digital structures.

Singh R. et al. (2020) designed a multilayer RAM cell. The design is utilizing a multiplexer, exclusive OR gate and D Latch. The circuit is efficient to provide read/Write and SET/RESET logic efficiently.

Naz et al. (2021) uses the loop-based structure to design 1X4 RAM. The design is 88% cost efficient than the existing RAM structures. The efficient 5-input MG based structure also includes decoder circuit.

Ahmadpour et al. (2021) designed a power efficient memory circuit. The design is multiplexer based with improvement in terms of area, cell count and power dissipation. The design is 4X1 and 8X1 multiplexer based.

Table 1 Comparison of Parallel RAM Cell and Serial RAM Cell

Metrix	Parallel RAM Cell Design	Serial RAM Cell Design
Memory Density	Less density	More Density
No. of QCA cells required	More	Less
CMOS circuit complexity	High	Low
Write/Read circuit	Duplicating for each bit	Sharing of bits in a loop
Latency	Low	High

6. Conclusion

Reconfiguration of memory circuits using Quantum Dot Cellular Automata will further improve the design in terms of power efficiency, read and write latency, area as well as cost. In parallel memory design, if clock signal duration will be different, we need time-to-space transformation by duplicating the circuit multiple times so as to form iterative logic array. In serial memory design, the clock time duration for all the four zones of semi-adiabatic switching must be different. Therefore, more than one clock is required for serial memory design. An improved design which can take the advantage of both parallel as well as serial memory architecture can be designed which must be more efficient in terms of no. of clock cycles, read and write latency, cell counts and wasted area over the existing designs.

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