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Energy Efficient 1- Bit Comparator Design in Quantum Dot Cellular Automata

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Abstract

Designing of digital circuits at nano level faces serious challenges like power dissipation, package density and physical barriers in CMOS. The researchers investigate other possible nanotechnologies having same capacities. Quantum Dot Cellular Automata (QCA) technology eliminates above said challenges. In this paper, QCA based single layer 1-bit comparator structure has been proposed. The proposed structure is efficient in occupational area, cell count, latency and Quantum Cost. The proposed comparator circuit has 0.24% improvement in cell count, 0.75% improvement in latency and 0.9% improvement in quantum cost. The energy dissipation analyses of proposed comparator have been calculated at tunneling energies of 0.5 Ek, 1.0Ek and 1.5Ek. The proposed comparator design dissipated4.98 % less energy at 0.5 Ek, 1.76 % less energy at 1.0Ek and 8.58 % less energy at 1.5Ek. as compared to the existing designs in literature. As a result, proposed designs are often found in various digital logics that require a small amount of space and low power consumption.

Keywords: Majority Gate, Comparator, QCADesigner, Energy Dissipation,

Abbreviations: Complementary metal Oxide Semiconductor (CMOS), Quantum Dot Cellular Automata (QCA), Tunneling Energy (TE), Majority Gate (MG)

1. Introduction

In CMOS there exist serious issues of leakage currents at nanoscale. These issues will be overcome in QCA nanotechnology with additional benefits like increased switching speed, reduced area and high energy efficiency [1]. Due to decreased feature size and power dissipation in CMOS results in higher device densities. But due to the scaling down of CMOS to submicron many limitations occur [2]. The challenges like un-deterministic leakage currents, quantum tunneling and short channel effects hinder the further scaling down process of CMOS circuits [3]. Hence the performance of CMOS devices deteriorates due to their rapid scaling down to nanometer range. Gordon Moore had mentioned in his article in that the scaling down of feature size can never be a continuous process [4]. The scaling down of a transistor channel length result in leakage currents due to quantum mechanical tunneling. Hence the performance of CMOS circuits degrades at such smaller scales.

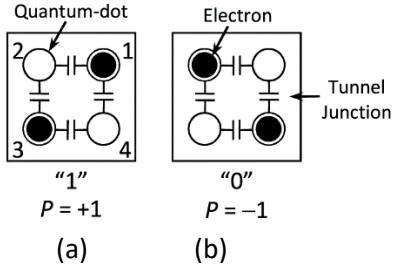
Instead of retaining the CMOS technology which causes serious limitations at the nano level, there is a need to devise an alternating approach that could overcome the above-said shortcomings. Dr. Criag S. Lent has proposed the QCA nanotechnologies in [5-6] at the University of Notre Dame. The primary unit of this nanotechnology is a QCA cell and its size is much smaller than the size of the smallest transistor. The QCA technology works on quantum mechanical tunneling that obstructs the CMOS operation at

nanoscale dimensions [7]. QCA is one such nano-computing platform that exploits some of the unavoidable nanoscale issues such as quantum effects and device integration for performing useful computation. In this research, two types of simulation tools have been used. One is QCA Designer tool and the other is QCAPro tool. QCA Designer tool [8] is used for designing proposed QCA circuits. Their structural analysis and simulations are done using QCA Designer tool. The energy dissipation of proposed design has been calculated with QCAPro tool at three different tunneling energies of 0.5 Ek, 1.0 Ek and 1.5 Ek.

2. Quantum dot Cellular Automata

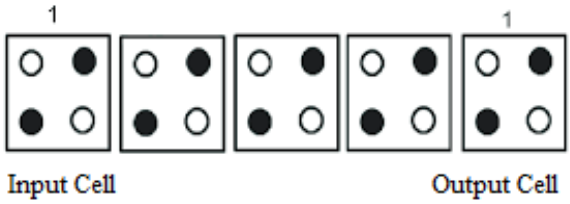
The fundamental unit in QCA nanotechnology is QCA cell [9]. It contains has four quantum dots with two electrons as depicted in Figure 1. The cell gets polarized when driven by clock signal. There are two polarization states of a cell, logic 1 and logic 0l. The positive polarization state is represented by logic 1 as shown in Figure 1(a) and the negative polarization state is represented by logic 0 in Figure 1(b). The logic state passes from input cell to output cell due to columbic interactions between the cells. The information is transmitted as columbic charge between the QCA cells which leads to energy efficient structures.

Figure 1 QCA Cell Polarization (a) Logic 1(P = +1) (b) Logic 0(p = -1) [9]



By connecting the cells in cascade, a QCA wire is formed [9]. The polarization that is logic 1 or logic 0 is formed by tunnelling of two electrons. This information is in the form of columbic charge only as depicted in Figure 2.

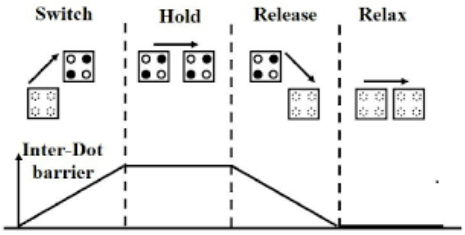
Figure 2 QCA Wire [9]



2.1 QCA Clocking

The QCA cell is polarized using clock signal shown in Figure 3. The purpose of clocking is to control the barrier between quantum dots to achieve a logic state [10]. There is a provision of four clocks for polarizing the circuit. Each clock utilizes four phases named as switch, hold, release and relax phase.

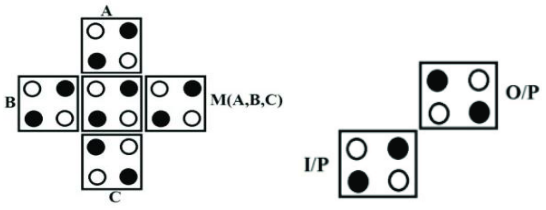
Figure 3 QCA Clocking [10]



2.2 QCA Basic Gates

There are two QCA gates named as 3-input MG and Not Gate is depicted in Figure 4. The QCA gates can be utilized to design any digital logic [11]. In the 3-input, majority of the inputs wins at the output whereas the NOT gate inverts the input state at the output.

Figure 4 QCA Gates (a) MG (b) NOT [11]



(a) (b)

3. Literature

The authors in [12] utilized reversible gates for developing a comparator design having a cell count of 73 and requires 0.06 µm2 area. The authors in [13] have developed a QCA comparator circuit without wire-crossing. The occupational area is about 0.055 µm2 area with 58 number of QCA cells. A Layered QCA comparator has been designed using basic gates in [14] having 0.038 µm2area with cell count of 44 with rotated QCA cells. A QCA comparator designed in [15] has 0.05 µm2area with 42 number of QCA cells. The area in [16] is 0.03 µm2 with total 38 cells. A comparator circuit in [17] requires 0.03 µm2area and 37 QCA cells. Another comparator in [18] has 37 cells and 0.75 clock delay with an occupational area of 0.06 µm2.The author in [19] designed a comparator circuit with 0.75 clock latency and having an area of 0.04 µm2 with 31 QCA cells. A comparator in [20] has 33 cells with 0.50 clock delay with an occupational area of 0.02 µm2. The comparator designs presented in literature are well suitable in performing their functions. But their performance can further be improved whose details are mentioned in next section.

4. Single - Bit Comparator Design

One of the main units of central processing unit is comparator circuit. It compares two logic states. A and B and generates three potential output signal which are ‘A>B’, ‘A=B’ and ‘A<B’. The basic block of a 1-bit comparator is depicted in Figure 5. Table 1 depicts the logical operation of a comparator circuit.

Figure 5 Block Diagram of Digital Comparator [12]

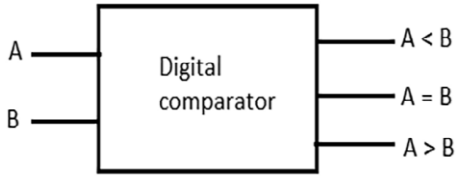


Table 1 Logic Operations of Comparator Circuit [12]

A	B	Y=A<B	Z=A=B	X=A>B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

The QCA cell geometry is given in Table 2.[21]

Table 2: QCA Cell Geometry

QCA Cell Geometry	
Cell Width	18nm
Cell Height	18nm
Dot Diameter	5nm
Center to Center Distance	20nm

4.1 Working and Simulation Output

The working of comparator circuit is explained with the help of Table 1. For the input combinations AB equals to either 00 or 11 then A = B at the output. This combination generated the operation of two input Ex-NOR gate. For the input combinations AB equals to 01 then A<B and for AB equals to 10 then A>B. The Boolean equations for all the above three cases are expressed as:

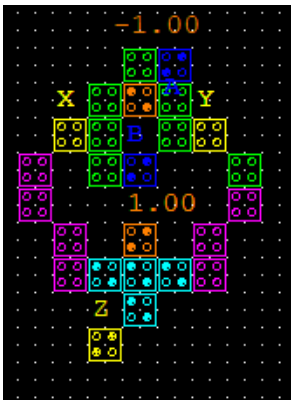
$$(A < B) = \bar{A}B \quad (1)$$

$$(A = B) = (AB + \bar{A}\bar{B}) = \overline{(\bar{A}B + A\bar{B})} \quad (2)$$

$$(A > B) = A\bar{B} \quad (3)$$

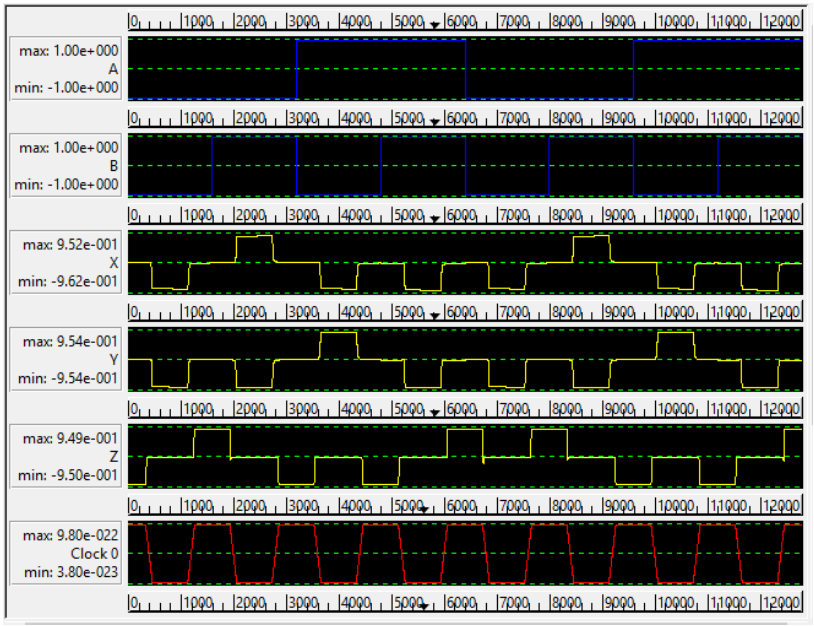
The proposed design in Figure 6 compares the 2- input bits ‘A’ and ‘B’ and produces three potential outputs ‘X’, ‘Y’ and ‘Z’. Where ‘X’, ‘Y’ and ‘Z’ represents ‘A>B’, ‘A<B’ and ‘A=B’ respectively.

Figure 6 Proposed 1-BitComparator Design



The simulations are done using QCA Designer tool. As illustrated in the figure 7 when the inputs A and B equals to logic 01 then A<B which can be shown by the output X, when the inputs A and B equals to logic 10 then A>B which is shown by output Y and inputs A and B equals to logic 00 or logic 11 then the inputs A=B which is shown by output Z.

Figure 7 Simulation Result of Proposed Comparator



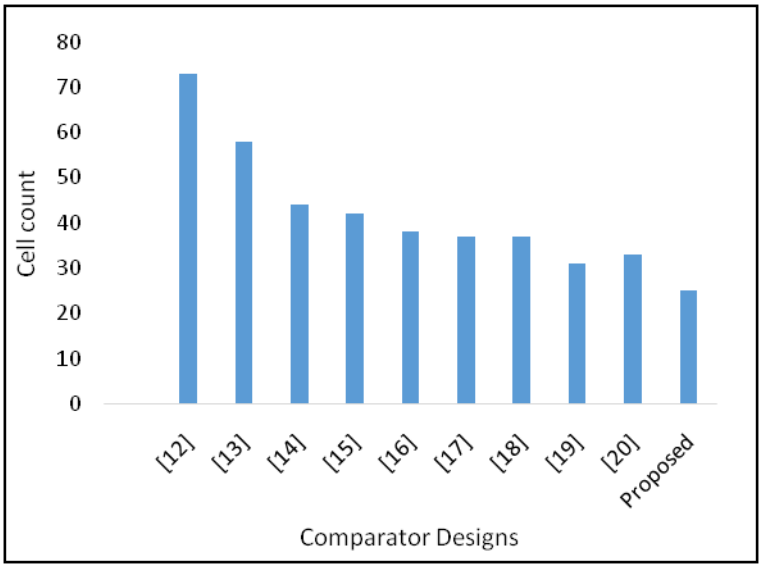
4.2 Performance Comparison of Proposed Comparator with Existing Designs

The structure of newly designed comparator has compared with the designs in literature as shown in Table 3. Various parameters considered for comparison are cell count, occupational area, latency and quantum cost. The proposed structure area occupation of 0.02 μm^2, having 25 number of cells, latency of 0.125 clock cycles and quantum cost of 0.002.

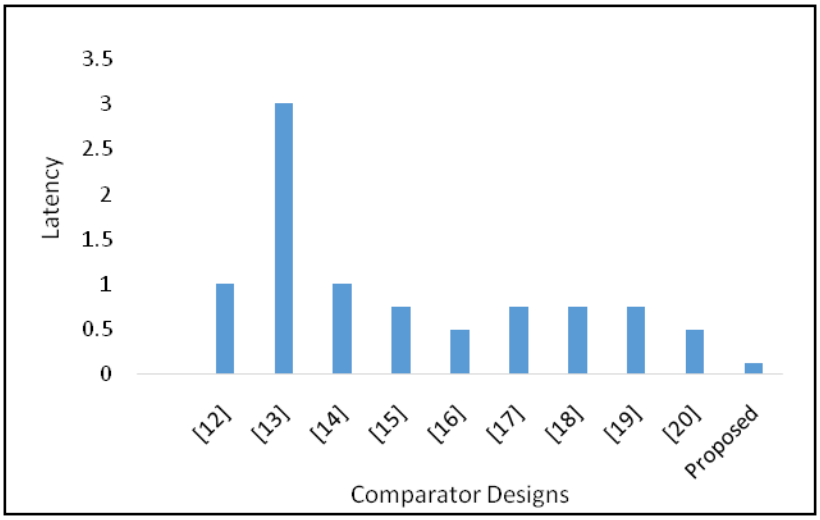
Table 3 Comparative Results of Proposed Comparator with the Designs in Literature

Design	Cell Count	Area (In μm^2)	Latency	Coplanar	Quantum Cost
[12]	73	0.06	1.0	Yes	0.053
[13]	58	0.055	3	Yes	0.028
[14]	44	0.038	1	Yes	0.038
[15]	42	0.05	0.75	Yes	0.022
[16]	38	0.030	0.50	Yes	0.015
[17]	37	0.03	0.75	Yes	0.013
[18]	37	0.06	0.75	Yes	0.006
[19]	31	0.04	0.75	Yes	0.026
[20]	33	0.02	0.5	No	0.020
Proposed	25	0.02	0.125	Yes	0.002

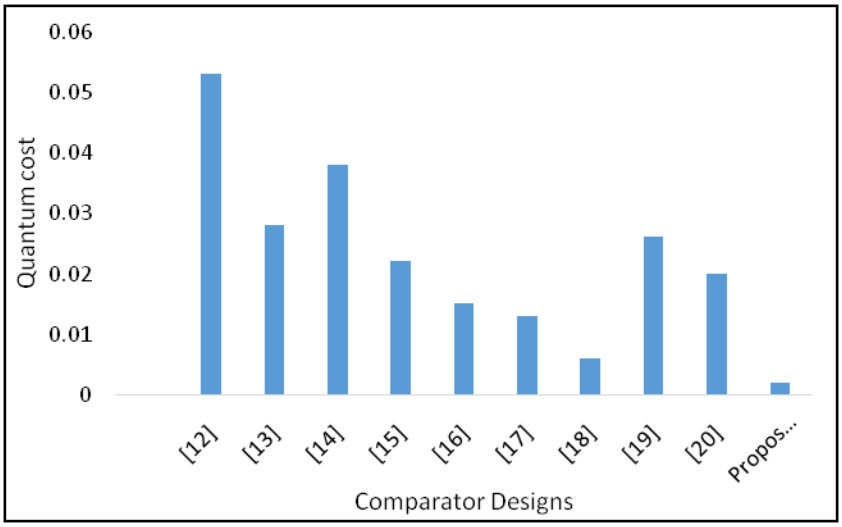
Figure 8 (a), (b), and (c) Graph Showing the Comparison of Cell Count, latency and Quantum Cost of Proposed Comparator with Existing Designs



(a)



(b)



(c)

The Figure 8 (a), (b) and (c) shows the comparative results of the proposed comparator with the designs in literature in terms of cell count, latency and quantum cost respectively. The proposed comparator design outperforms the existing designs mentioned in literature. Hence, the proposed comparator has 0.24 % improvement in cell count, 0.75% improvement in latency and 0.9% improvement in quantum cost.

5. Energy Dissipation Analysis

When the clock is given to the input of a cell, it gets polarized to either logic 1 or 0 state. This logic state travels from input to the output cell via device cells. During the columbic interactions between the cells, some amount of power is dissipated [21]. Hence, the power dissipation in QCA is considered as one

of the important parameters for designing digital circuits at the nano level. The power to the QCA circuit is provided by means of clock energy which raises or lowers the potential barriers in a QCA cell. In QCA, non-adiabatic power loss is considered. From the quasi-adiabatic model, the energy of a QCA cell is given by

$$\boldsymbol{E} = \frac{\hbar}{2}.\vec{\boldsymbol{\Gamma}}.\vec{\boldsymbol{\lambda}} \tag{4}$$

Here, ħ = Plank's Constant = 6.626176 x 10-34 joule-seconds.

(λ) $^{\rightarrow}$=coherence energy vector Γ $^{\rightarrow}$=3D vector

The QCA cell Instantaneous Power is given as,

$$P_{total} = \frac{d\boldsymbol{E}}{dt} = \frac{d}{dt}\left[\frac{\hbar}{2}.\vec{\Gamma}.\vec{\lambda}\right] \tag{5}$$

$$P_{total} = \frac{\hbar}{2}\left[\frac{d\vec{\Gamma}}{dt}.\vec{\lambda}\right] + \frac{\hbar}{2}\left[\vec{\Gamma}.\frac{d\vec{\lambda}}{dt}\right] \tag{6}$$

$P_{total} = P_1 + P_2$,

The first term i.e. $P_1 = \frac{\hbar}{2}\left[\frac{d\vec{\Gamma}}{dt}.\vec{\lambda}\right]$is divided in two parts, Power transferred from clock to a cell and the difference in power gain. Here, $P_2 = \frac{\hbar}{2}\left[\vec{\Gamma}.\frac{d\vec{\lambda}}{dt}\right]$ is an instantaneous power dissipation. The energy dissipated by a cell during its switching in the single clock is:

$$E_{diss} = \int_{-T}^{T} P_2\, dt = \frac{\hbar}{2}\int_{-T}^{T} \vec{\Gamma}.\frac{d\vec{\lambda}}{dt}\, dt \tag{7}$$

The energy estimation tool named QCAPro is used to calculate the energy of a circuit [22]. Average Leakage energy loss occurs at clock transitions i.e. when the clock is at raising or lowering edge. During the clock transition, the QCA cell will either get polarized or depolarized. Average switching energy loss occurs when the QCA cell changes its state as soon as the clock is applied. Hence the three events where the energy loss occurs in QCA are during i) Switching phase of the clock, where a cell remains to depolarize, ii) holding phase where the cell is fully polarized, iii) release and relax phase where there is depolarization of a cell occurs. Above mentioned events are related to an energy loss. The first and third event is related to average leakage energy loss whereas the second event relates to average switching energy loss [23].

5.1 Simulation Setup

The Purpose of designing a Comparator Circuit using QCA technology is to minimize its energy dissipation so as to make it power efficient. QCAPro tool is a simulator which is designed to estimate non-adiabatic energy dissipation of QCA structures [24]. The QCAPro tool has been installed on a Linux based environment, fedora 10. The tool requires three files as the input: .qca file from QCA Designer tool, vector file containing all the possible input and output combinations and the switching vector file which contains all the possible input combinations of proposed designs. Here, .qca file is obtained from QCA Designer

tool that contains the proposed QCA majority structure. Both the vector set file and the switching vector file are the text files. These text files are made manually using a notepad on a Linux based environment

5.2 Comparative Energy Dissipation Analysis of Proposed Comparator Design with Existing Designs

Here, three types of energy dissipations that is switching, leakage and average energy have computed at the tunneling energies of 0.5 Ek, 1.0Ekand 1.5Ek. Tables 2, 3 and 4 given below compares the three energy dissipations of proposed comparator with the existing design. The results shows that all the three energy dissipations for the proposed comparator design are lesser than the designs in literature.

5.2.1 Comparative Average Energy Dissipation Analysis

Tables 4, 5 and 6 shows the comparison of all the three energy dissipations for the proposed comparator and existing designs. From the comparison tables, it is clear that all the three energy dissipations for the proposed comparator design are lesser than the designs in literature.

Table 4 presents the comparison of average leakage energy dissipation and Fig 9 shows their comparison in the form of a bar graph. It is clear that the average leakage energy dissipation of new comparator at0.5Ek is 10.1 meV which is 0.090 % less, at1.0Ek is 25.6 meV, which is 0.003 % less, at 1.5Ek is 42.5 meV, which is 0.109 % less than the best-reported design.

5.2.2 Comparative Switching Energy Dissipation Analysis

Table 5 and Figure 10 shows that the switching energy dissipation of new comparator at0.5Ek is 28.0 meV which is 0.034 % less, at1.0Ek is 24.5 meV, which is 0.057 % less, at 1.5Ek is 21.4 meV, which is 0.036 % less than the best-reported design.

5.2.3 Total Energy Dissipation Analysis of Proposed Comparator with Existing Designs

Table 6 and Figure 1 shows that the switching energy dissipation of new comparator at0.5Ek is 38.1 meV which is 0.049 % less, at1.0Ek is 50.1 meV, which is 0.017 % less, at 1.5Ek is 63.9 meV, which is 0.085 % less than the best-reported design.

Table 4 Comparative Analysis of Average Leakage Energy Dissipation of Proposed Comparator with Existing Designs at Three Tunneling Energies

Comparator Design	Average Leakage Energy Dissipation in meV		
↓ Design\ TE →	0.5 E_k	1.0 E_k	1.5 E_k
[12]	18.41	56.1	101.3
[13]	17.0	56.0	101.1
[14]	13.42	55.13	75.25
[15]	13.40	38.6	67.3
[16]	13.00	38.5	66.5
[17]	12.5	36.2	62.8
[18]	11.45	34.12	60.43
[19]	11.4	31.6	53.8
[20]	11.1	25.7	47.7
Proposed	10.1	25.6	42.5

Figure 9 Graph Showing the Average Leakage Energy Dissipation of Proposed Comparator and Existing Designs at Three Tunneling Energies

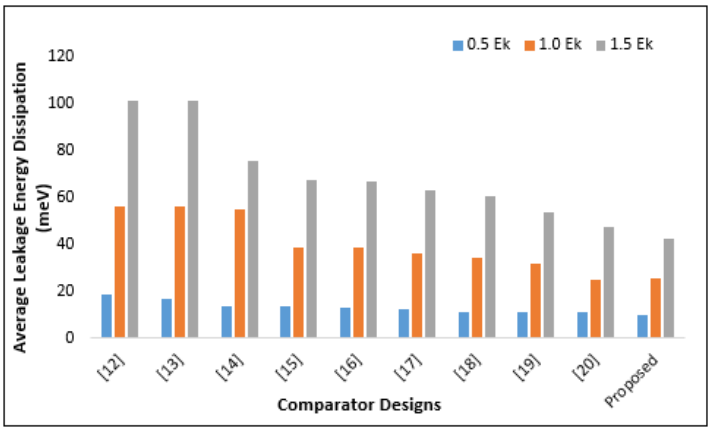


Table 5 Comparative Analysis of Switching Energy Dissipation of Proposed Comparator with Existing Designs at Three Tunneling Energies

Comparator Design	Average Switching Energy Dissipation in meV		
↓Design\ TE →	0.5 E_k	1.0 E_k	1.5 E_k
[12]	62.3	56.7	50.5
[13]	57.7	55.3	38.8
[14]	57.16	53.14	38.30
[15]	53.6	45.7	38.1
[16]	38.5	32.3	27.0
[17]	36.0	33.7	26.4
[18]	35.8	32.38	26.3
[19]	30.1	26.6	23.0
[20]	29.0	26.0	22.2
Proposed	28.0	24.5	21.4

Figure 10 Graph Showing Average Switching Energy Dissipation of Proposed Comparator and Existing Designs at Three Tunneling Energies

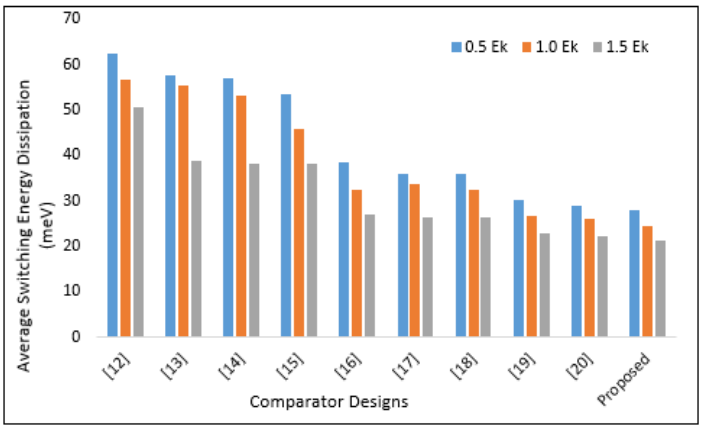
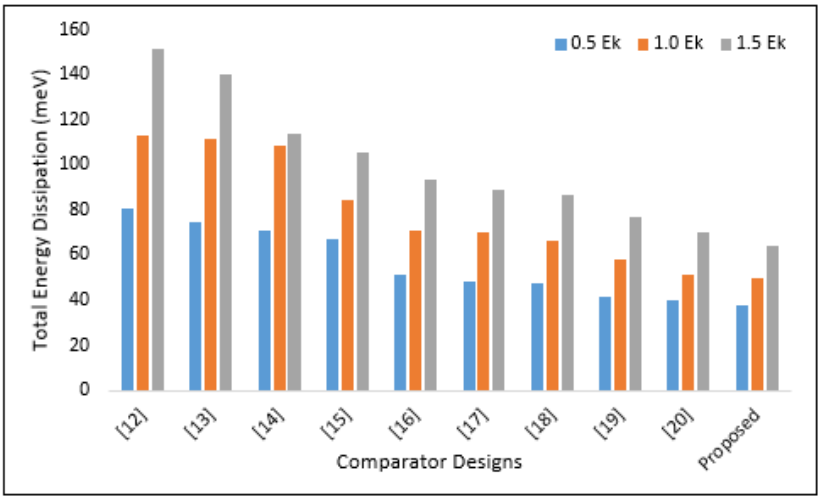


Table 6 Comparative Analysis of Average Energy Dissipation of Proposed Comparator with Existing Designs at Three Tunneling Energies

Comparator Design	Total Energy Dissipation in meV		
↓ Design\ TE →	0.5 E_k	1.0 E_k	1.5 E_k
[12]	80.71	112.8	151.8
[13]	74.7	111.3	139.9
[14]	71.02	108.27	113.55
[15]	67.0	84.3	105.4
[16]	51.5	70.8	93.5
[17]	48.5	69.9	89.2
[18]	47.25	66.5	86.73
[19]	41.5	58.2	76.8
[20]	40.1	51.0	69.9
Proposed	38.1	50.1	63.9

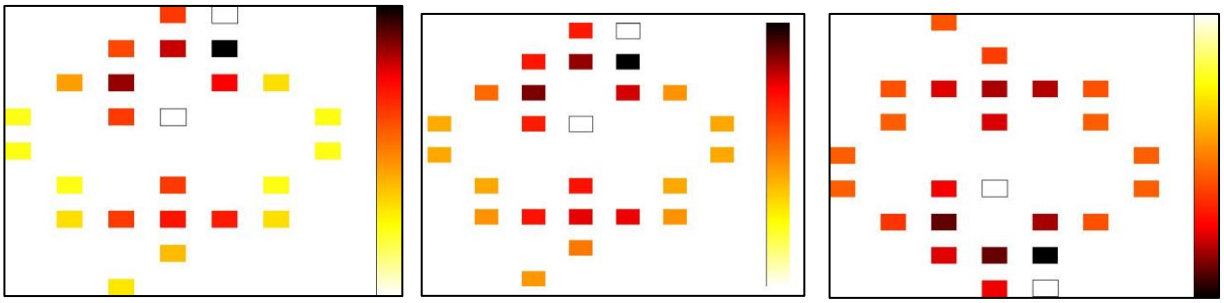
Figure 11 Graph Showing Average Energy Dissipation of Proposed Comparator and Existing Designs at Three Tunneling Energies



6. Thermal Map of Proposed Comparator

From the thermal map of proposed comparator circuit, it is concluded that as the tunneling energy increases from 0.5Ek to 1.5 Ek, the thermal energy dissipation also increases [26]. Which means that at a higher value of tunneling energy i.e. 1.5 Ek, the thermal dissipation is more. Whereas for the lower value of tunneling energy i.e. at 0.5Ek, the thermal dissipation is less. Hence the value of tunneling energy should keep minimum for low power dissipation. It is important to note about the kink energy that it depends on the dimensions as well as the spacing between the QCA cells [27-28].

Figure 12 Thermal Map of Proposed Comparator Circuit at (a) 0.5Ek (b)1.0 Ek (c)1.5 Ek



(a) (b) (c)

7. Results and Conclusion

Reconfigurability of a comparator design with QCA will add a new dimension, as the area is reduced considerably with low implementation cost due to the absence of multilayer, rotated and diagonal QCA cells in the design. Hence comparator design in QCA nanotechnology is chosen for the improvement in parameters like a number of cells, occupation area, quantum cost and hence energy dissipation. The results concludes that the average energy dissipation is minimum at the tunneling energy of 0.5 Ek and is maximum at tunneling energy of 1.5 Ek.

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