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Energy Dissipation Analysis of Sequential Circuits in QCA

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Abstract

There are lot of alternate technologies in recent years at nano-scale to replace the conventional CMOS technology. Among the new devices, Quantum-dot Cellular Automata (QCA) is one such technology that relies on new physical phenomena called Columbic interactions. QCA is a nanotechnology that radically departs from a CMOS-based technology in terms of energy dissipation, occupational area and input to output delay. In this paper, the sequential circuits such as SR latch and D Latch has been designed with the help of QCA software. The simulation result shows that the proposed SR latch utilizes an area of 0.01 μm^2 with 72 QCA cells and a delay of 2 clock cycles. Similarly, the proposed D latch has occupational area of 0.04 μm^2 with 29 QCA cells and a delay of 1 clock cycle. The average energy dissipation of both the latches has been calculated at 0, 5, 10 and 15 Kelvin (K). The average energy dissipation of proposed SR latch at 0Kis 0.06212 meV, at 5K is 0.1574 meV, at 10K 0.09411 meV is and at 15K is 0.08988 meV. Similarly, the average energy dissipation of proposed D latch at 0K is 0.0257 meV, at 5K is 0.07066 meV, at 10K is 0.06987 meV and at 15K is 0.06713 meV

INTRODUCTION

From the past five decades, the conventional Complementary Metal Oxide Semiconductor (CMOS) paradigm follows Moore's Law, where the number of devices on a single chip double in every 18 months [1]. This trend results in decreased feature size and power dissipation with higher device densities. But due to the scaling down of CMOS to submicron, many limitations occur. The challenges like un-deterministic leakage currents, quantum tunneling and short channel effects hinder the further scaling down process of CMOS circuits. Hence the performance of CMOS devices deteriorates due to their rapid scaling down to nanometer range. Gordon Moore had mentioned in his article in that the scaling down of feature size can never be a continuous process. The scaling down of a transistor channel length result in leakage currents due to quantum mechanical tunneling. Hence the performance of CMOS circuits degrades at such smaller scales.

Instead of retaining the CMOS technology which causes serious limitations at the nano level, there is a need to devise an alternating approach that could overcome the above-said shortcomings. Dr. Criag S. Lent has proposed one of the nanotechnologies in called as Quantum-dot Cellular Automata (QCA) at the University of Notre Dame. The primary unit of this nanotechnology is a QCA cell and its size is much smaller than the size of the smallest transistor. The QCA technology works on quantum mechanical tunneling that obstructs the CMOS operation at nanoscale dimensions. Today's generation multimedia products which are based on embedded system design with system on chip requires very high performance in terms of occupation area, clock delay and energy dissipation. The sequential circuits of embedded design with system on chip strongly effect the performance of the system [2]. Sequential circuits [3] are the essential elements of today's technology. Any processor that is designed using a semiconductor technology utilizes [4] the sequential circuits as a part of the chip design. As observed by Moore's Law there is a trend of doubling the total number of transistors on the die after every year. Intel technology with 32nm can incorporate 1.9 billion transistors in SRAM [5]. This exponential trend of scaling down of chip area is achieved only by VLSI technology. Current CMOS technology is facing the limitations of leakage currents, doping fluctuations and short channel effects which prevent the further decrease in feature size. It is projected that the scaling down of chip area of known-today CMOS technique will end at the channel length of 7 nm by 2024 [6].

There are lot of alternate technologies in recent years at Nano-scale to replace the conventional CMOS technology. Nanotechnologies have a unique feature of reduced area occupation that provides the opportunities for the researchers to explore at such a reduced feature size [7-8]. Quantum-dot Cellular Automata is one such nano-technology which utilise the new physical phenomena (of Columbic interactions between the electrons in a cell), that is totally different from a CMOS-based technology [9-10]. QCA gives an opportunity to compute at Nano-level. In CMOS systems some circuits perform computation while others circuits (wires perform signal/data transfer. In contrast, computation and communication occurs simultaneously in QCA which results in decrease in feature size [11-12]. The author in presented a Line-Based [13-14] QCA Memory Cell Design with improvement in Area, Complexity and Throughput [15]. The author in [16] proposes a memory cell design with the improvement in energy consumption, design complexity and higher speed. Author in [17] Proposes SRAM design with improved area occupation, circuit complexity, latency, throughput and energy dissipation.

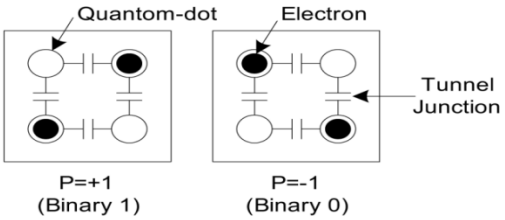
QUANTUM DOT CELLULAR AUTOMATA

QCA is the novel nano-technology that was introduced in 1993. In QCA, the binary levels are not depicted as +V or –V volts but they are saved as the placement of individual electron in a QCA cell. Bistable charge configuration is used in QCA to represent the binary states. A QCA cell contains four quantum dots that are placed at an extreme corner of a qca cell. The charge in it is placed in the form of a quantum dot. It is made up of compound semiconductor material such as gallium arsenide etc. The construction of basic QCA cell is discussed in next section.

Fundamentals Logics in QCA

A cell is the fundamental element in Quantum dot Cellular Automata. Each cell is representing a binary logic by an appropriate configuration of electron charge as presented in Figure 1. It contains four quantum-dots. Each quantum dot [18] is made up of a semiconductor nano-material that shows quantum-mechanical effects. The two out of the 4 dots occupying electrons in a “diametrically opposite” locations. These electrons are placed at the opposite corner (diagonal) of a QCA cell because the Coulomb repulsion in a diagonal position is less as compared to an adjacent position. The coupling of quantum dots is done by tunnel junctions.

Figure 1. QCA Cell and Two Polarization States. [18]

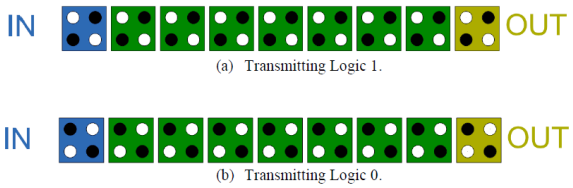


The tunnelling [19] between the electrons can takes place only by applying the potential to the QCA cell otherwise they are not able to leave the dot. An important feature in QCA is that an electron can never leave its QCA cell, hence reducing the energy dissipation of a circuit. The tunnelling phenomenon of tunnel junctions are shown in Figure 1. The electrons positioned at the corners depicts the two ground-state polarization (P = +1 and P = -1) levels.

QCA Wire (90 degree)

The cells can be placed in adjacent to each other to form a wire. The electrostatic force between the cells helps the electrons to occupy their positions within the cell. The position of an electron within a QCA cell depicts the logic state as presented in Figure 2. This logic level can be moved to the output QCA cell along with a QCA wire is due to the polarization between the adjacent cells.

Figure 2. QCA Wire [18]

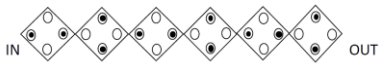


The binary logic state propagates from the left-hand side to the right-hand side via columbic interactions between QCA cells. The QCA cells connected in cascade will follow the charge configuration of their previous adjacent cell. Hence this creates a binary logic state at the output cell.

QCA Wire (45 degree)

The QCA wire (45 degree) having an orientation of 45^0 [18] can transfer the logic state which switches alternatively between P = +1 and P = -1 polarization for every QCA cell connected in cascade as shown in Figure 3. The main advantage of QCA 45^0wire is that it transfers the logic state without the use of an inverter circuit.

Figure 3. QCA Wire 45 Degree [19]

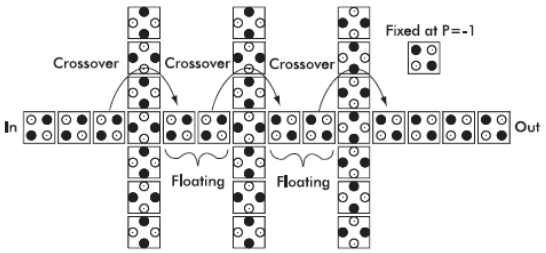


QCA Wire Crossing

In CMOS circuits, the wire crossings are formed by making a bridge from the plane and the signal is in the form of voltages and currents. However, in QCA the logic states can cross each other at the same plane. The main rule for wire crossover design in QCA is that if one of the wires is a simple binary wire than the other should be an inverted wire.

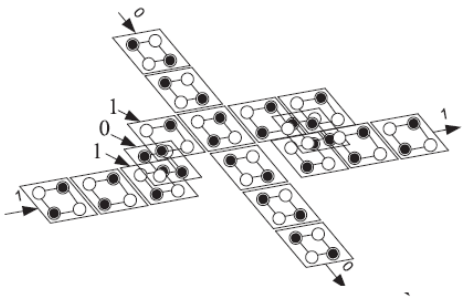
The two types of QCA wire crossing are i) coplanar ii) multilayer. A coplanar wire crossing is designed on a single layer as shown in Figure 4. Here horizontal axis utilizes regular QCA cell and vertical axis uses rotated QCA cells. Both types of QCA cells do not interfere with each other. The main disadvantage of such type of wire crossing is a misalignment of QCA cells.

Figure 4. A Section of Wire with Three Wire Crossings [19]



Whereas multilayer wire crossing structure uses another layer for interconnection [19]. To connect the signal to the desired layer by using cross over, the QCA cells needs to be stacked on one another in a vertical direction to reach to the desired layer. As the signal reaches the desired layer, it again transmits in the horizontal direction as illustrated in Figure 5. The main advantage of multilayer cross over design is that they occupy lesser area as compared to coplanar design. Such circuits have more stable simulations as compared to coplanar design. However, these structures are very difficult to fabricate and are very expensive in comparison to coplanar designs.

Figure 5. A Multi-Layer Crossover Wire [19]



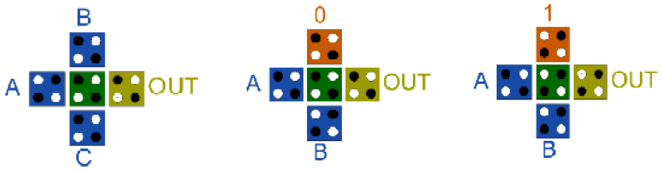
Logic Gates in QCA

The construction of Majority gate is depicted in Figure 6(a). As its name indicates, the majority of the inputs wins at the output, for example if '100' is applied to inputs A, B, C then output obtained is '0' which represents the majority of inputs [20]. The expression for the output of the Majority voter is:

$$M(A, B, C) = AB + BC + AC$$

AND Gate and OR gate can be designed using majority gate. By connecting any one of the three inputs (say C) to 0, the majority voter can act as an AND gate (Figure 6b). Similarly, if all the three inputs are set to 1, the majority gate can now work as an OR gate (Figure 6c).

Figure 6: Construction of Majority, AND, OR Gate [20]

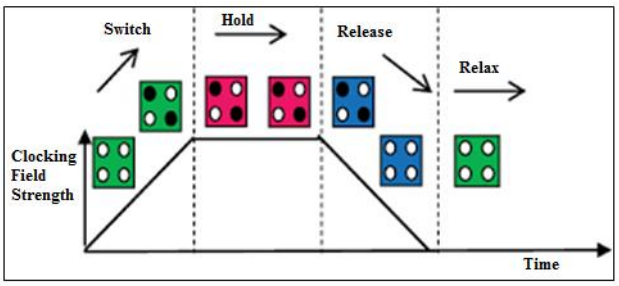


(a) Majority Gate **(b) AND Gate** **(c) OR Gate**

QCA CLOCK THEORY

The synchronization of information in a QCA circuit is controlled by a clocking mechanism [28]. A QCA clock has 4 clock phases: Switch, Hold, Release and Relax phase as shown in Figure 7.

Figure 7. Four Phases of a QCA Clock [21]



When the clock signal is applied to a QCA cell, it undergoes all the four phases of a clock. In switch phase, the clock field strength starts increasing and the cell starts polarizing. When the QCA cell is in hold phase, the field strength is maximum and the cell gets fully polarized. In this phase, the QCA cell will attain its logic state '0' or '1'. In release phase, the clock field strength starts decreasing and the QCA cell will start depolarizing. In relax phase, field strength is minimum and QCA cell gets fully depolarized. [25]

PRESENTED QCA SR-LATCH AND D-LATCH

Latch is a basic memory component used to store one bit at a time [21-22]. The QCA equivalent of SR Latch and D Latch is shown in Figure 8 and 9. From Figure 8, it is clear that the SR latch will sets the output to logic 1 when Set pin is at high state. Similarly, the SR latch resets the output to logic 0 when Reset pin is at low state. The D Latch has single input i.e., D input. The D latch will set the output to logic 1 when the D Input is at logic 1. The QCA structure of D latch is depicted in Figure 9. Table 1 represents the coherence engine simulation parameters taken for simulation.

Table 1. Coherence engine simulation Parameters

Parameter	Value
Width of QCA cell (nm)	18
Height of a cell (nm)	18
Diameter of Quantum – Dot	5
Time for Relaxation (in seconds)	1.0e-15
Total Time for Simulation (in seconds)	7.0e-11
Amplitude factor of the Clock	2.0

Figure 8. QCA Implementation of SR latch Structure

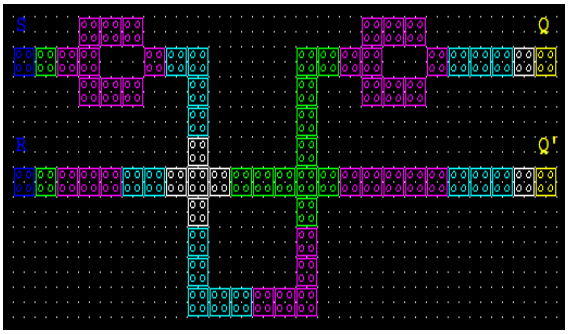
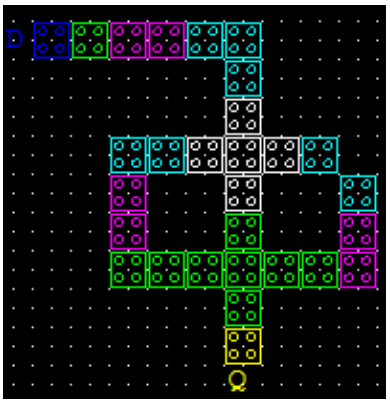


Figure 9. QCA Implementation of D latch Structure



SIMULATION RESULTS

QCA is one such nano-computing platform that exploits some of the unavoidable nanoscale issues such as quantum effects and device integration for performing useful computation. In this paper, two types of simulation tools have been used. One is QCADesigner tool and the other is QCAPro tool. QCADesigner tool is used for designing proposed QCA circuits. Their structural analysis and simulations are done using QCADesigner tool. For energy dissipation

Figure 10. Simulation-Output of a Presented SR Latch

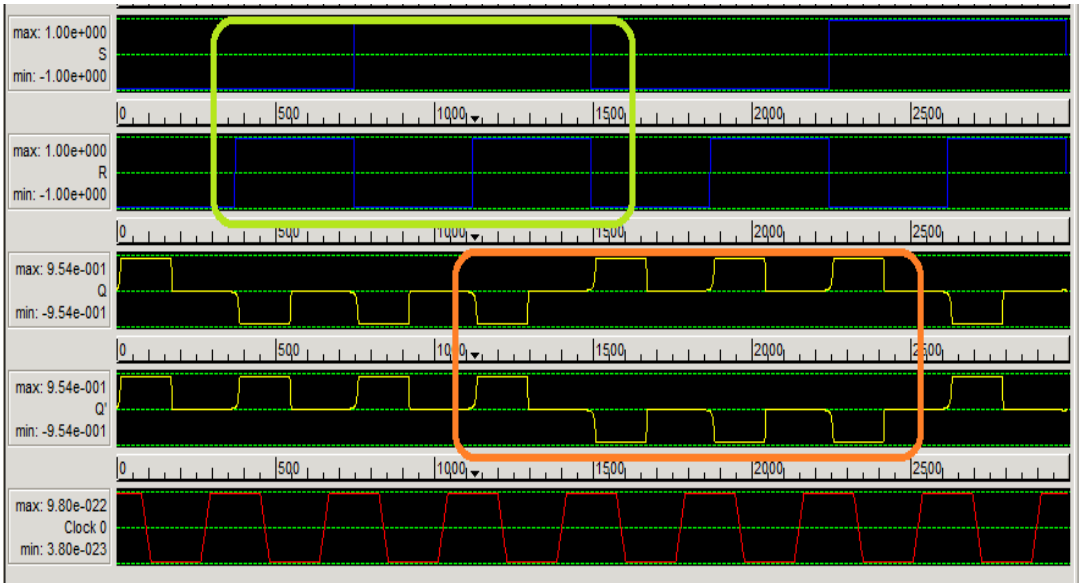
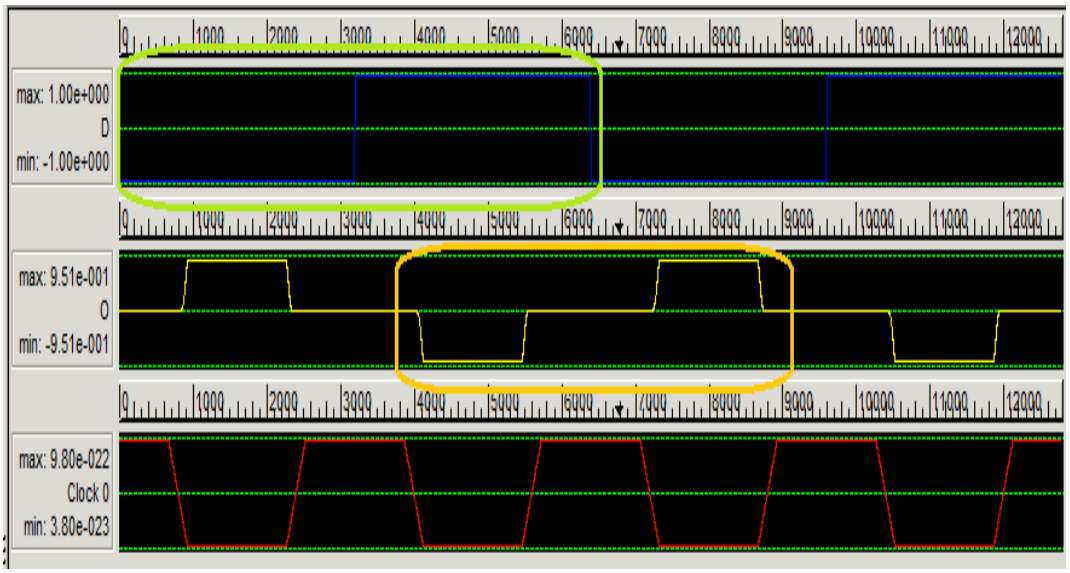


Figure 11: Simulation-Output of a Presented D Latch



analysis of proposed designs, QCAPro tool has been used. With this tool, average leakage energy, average switching energy and average energy dissipation of a QCA design have been analyzed at three different temperatures i.e., zero, 5, 10 and 15 Kelvin. The design verification of SR latch and D Latch [23] is being done by using QCADesigner 2.0.3 simulation is depicted in Figure 10 and 11. The comparison results Table 3 depicts that the total latency of an SR latch is 2 clock cycles and the latency of D latch is 1 clock cycle [24-25].

THERMAL LAYOUT AND ITS ENERGY DISSIPATION ANALYSIS

When the clock is given to the input QCA cell of a proposed majority gate, it gets polarized to either logic 1 or 0 state. This logic state travels from input to the output cell via device cells. During the columbic interactions between the cells, some amount of power is dissipated. Hence the power dissipation in QCA is considered as one of the important parameters for designing digital circuits at the nano level. The power to the QCA circuit is provided by means of clock energy which raises or lowers the potential barriers in a QCA cell. In QCA, non-adiabatic power loss is considered. Low power dissipation, even below traditional KT, is one of the main features of this nanotechnology. The basic concept is taken from the quasi-adiabatic model in [26]. According to this model, the expectation energy value of the cell for every clock cycle is described as

$$E = \frac{h}{2}.\vec{\Gamma}.\overrightarrow{\lambda} \quad (1)$$

Here, ħ = Plank's Constant = 6.626176 x 10^{-34} joule-seconds.

$\overrightarrow{\lambda} = \text{coherence vector}$

$\vec{\Gamma} = 3\text{D energy vector}$

Now, QCA cell power at any instant is given as Instantaneous Power,

$$P_{total} = \frac{d\mathbf{E}}{dt} = \frac{d}{dt}\left[\frac{\hbar}{2}.\vec{\Gamma}.\vec{\lambda}\right] \quad (2)$$

$$P_{total} = \frac{\hbar}{2}\left[\frac{d\vec{\Gamma}}{dt}.\vec{\lambda}\right] + \frac{\hbar}{2}\left[\vec{\Gamma}.\frac{d\vec{\lambda}}{dt}\right] \quad (3)$$

$$P_{total} = P_1 + P_2 \quad (4)$$

The first term i.e.,$P_1 = \frac{\hbar}{2}\left[\frac{d\vec{\Gamma}}{dt}.\vec{\lambda}\right]$ indicates two components, first is the transfer of power generated from clock to QCA cell and the second is power gain difference due to input and output power. The second term $P_2 = \frac{\hbar}{2}\left[\vec{\Gamma}.\frac{d\vec{\lambda}}{dt}\right]$is instantaneous power dissipation. The energy dissipated by a cell during its switching in the single clock is calculated by integrating the term P_2over time as:

$$E_{diss} = \int_{-T}^{T} P_2\, dt = \frac{\hbar}{2}\int_{-T}^{T} \vec{\Gamma}.\frac{d\vec{\lambda}}{dt}\, dt \quad (5)$$

The value of energy dissipation is maximum for the maximum changing rate of$\vec{\Gamma}$. The average energy dissipation in a QCA design is categorized as average leakage energy dissipation, average switching energy dissipation. The sum of above two energies is the average energy dissipation. The energy estimation tool named QCAPro is used to calculate the energy dissipation of a circuit. Average Leakage energy loss occurs at clock transitions i.e., when the clock is at raising or lowering edge. During the clock transition, the QCA cell will either get polarized or depolarized. Average switching energy loss occurs when the QCA cell changes its state as soon as the clock is applied. Hence the three events where the energy loss occurs in QCA are during i) Switching phase of the clock, where a cell remains to depolarize, ii) holding phase where the cell is fully polarized, iii) release and relax phase of the clock where the cell again comes back to the depolarized state. Above mentioned events are related to an energy loss. The first and third event is related to average leakage energy loss whereas the second event relates to average switching energy loss. Hence according to the definition, leakage energy dissipation is the energy loss during clock transitions at the leading edge or trailing edge of the clock pulse and switching energy dissipation occurs during the switching state of a QCA cell over a clock cycle. The Hamiltonian matrix is used to calculate the average energy dissipation.

$$E_{ij} = \begin{bmatrix} \frac{-E_k}{2}\sum iC_i f_{i,j} & -\gamma \\ -\gamma & \frac{-E_k}{2}\sum iC_i f_{i,j} \end{bmatrix} \quad (6)$$

$$E_{ij} = \begin{bmatrix} \frac{-E_k}{2}\sum C_{j-1} + C_{j+1} & -\gamma \\ -\gamma & \frac{-E_k}{2}\sum C_{j-1} + C_{j+1} \end{bmatrix} \quad (7)$$

Where, C_i is ith cell polarization, F_{ij} is geometrical-factor representing the columbic interaction between the cells due to the distance. eK is kink energy. Table 2 presents the average energy dissipation of SR and Table 3 presents

the average energy dissipation of D latch. From Table 2, it is clear that the average energy dissipation of proposed SR latch at 0K is 0.06212 meV, at 5K is 0.1574 meV, at 10K 0.09411 meV is and at 15K is 0.08988 meV.

Table 2. Average Energy Dissipation of SR Latch in meV

Temperature (in Kelvin)	Average Energy Dissipation of SR Latch (meV)
0	0.06212
5	0.07741
10	0.08988
15	0.09411

The average energy dissipation of both the latches has been calculated at 0, 5, 10 and 15 Kelvin (K). From Table 3, it is clear that the average energy dissipation of proposed D latch at 0K is 0.0257 meV, at 5K is 0.07066 meV, at 10K is 0.06987 meV and at 15K is 0.06713 meV.

Table 3. Average Energy Dissipation of D Latch in meV

Temperature (in Kelvin)	Average Energy Dissipation of D Latch (meV)
0	0.0257
5	0.06187
10	0.07066
15	0.08713

Figure 12 and 13 represents the temperature verses energy dissipation graphs of SR and D latch. From the graphs it has been proved that the energy dissipation of both the latches increases with the increase in temperature.

Figure 12. Average Energy Dissipation of SR – Latch

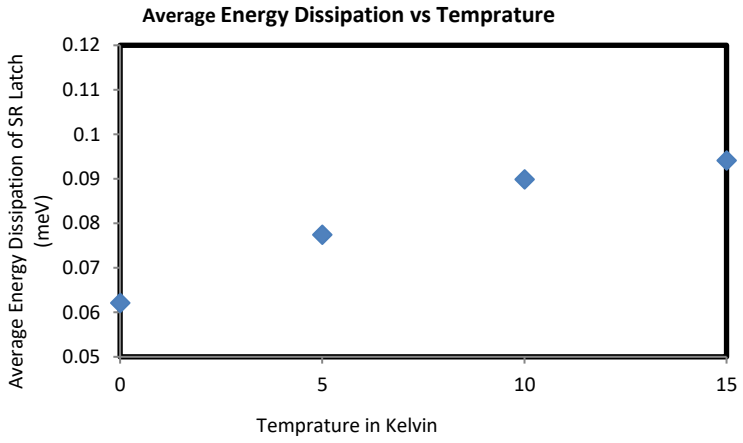
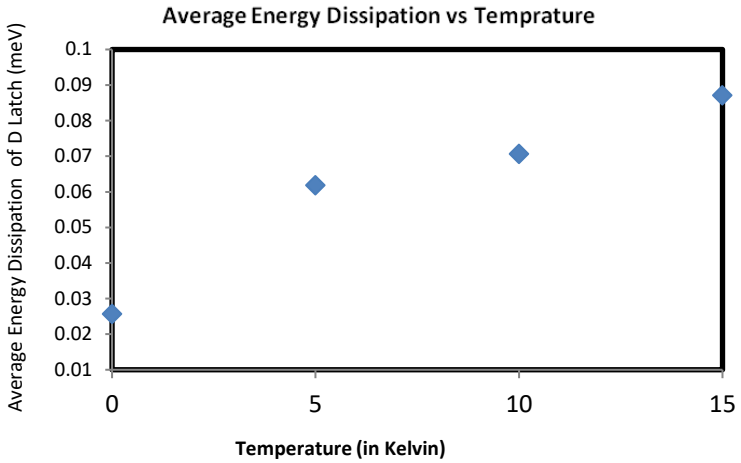
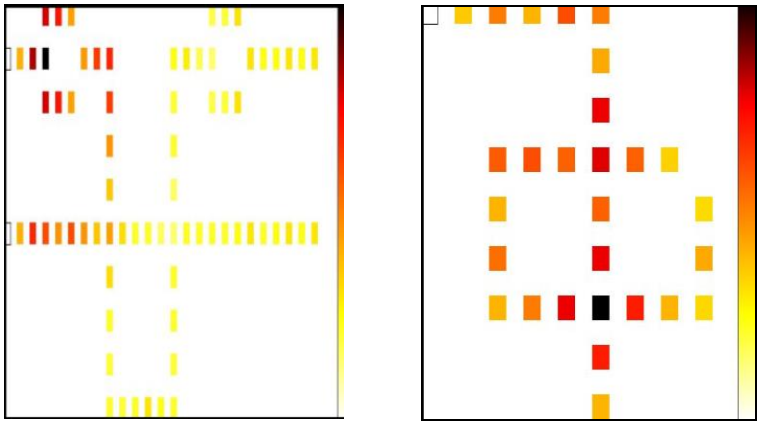


Figure 13. Average Energy Dissipation of D – Latch



The thermal views of both the latches are depicted in Figure 14. The dark colored QCA cell represents more heat dissipation in comparison to the lighter colored QCA cell.

Figure 14.: Thermal View of the Average Energy Dissipation in each cell at 5k (a) SR Latch (b) D Latch



(a) (b)

The comparison results of both the latches in terms of total number of QCA cells, occupation area and latency are depicted in Table 4.

Table 4. Parameters of SR and D Latch

S No	Circuit	No. of cells	Circuit Area(μm^2)	Latency
1	SR Latch	72	0.01	2 clock cycles
2	D Latch	29	0.04	1 clock cycle

CONCLUSION

Reconfiguration of memory circuits using nanotechnology such as QCA is analyzed. Structural and Energy dissipation analysis is performed on SR and D latch. The simulation result shows that the SR latch is occupying an area of 0.01 μm^2, 72 number of QCA cells with the latency of 2 clock cycles. Similarly, a D-latch is occupying an area of 0.04 μm^2, 29 number of QCA cells with a latency of 1 clock cycle. Average energy dissipation of SR and D latch increases with the increase in temperature. The design of a memory structures with reduced cell count has enhanced its area optimization capabilities and energy efficiency. So, it finds wide applications in the electronics industry. Hence in future QCA will have a broad spotlight on strategies for proficient routing interconnect and more precise timing models to reproduce the efficient digital designs.

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