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Isolation Polarity Check In UPF Design Using Clamp Checker

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Abstract: Low Power Aware verification became a major concern in the semiconductor industry. The shrinking size of the engineers allowed several approaches to be applied. This has made the process of verifying thepower aware constraints for the design complicated. To approach the power aware verification for complex designs in 2007. Accellera introduced Unified-Power-Format (UPF) (1.0) standards. Later in 2009, IEEE introduced standard UPF 2.0 format which enabled the verification engineers to use inbuild and static and dynamic rules which can be used for validating the power intents and the given specifications of the design.UPF is predominantly used for defining power management and methods which are used for minimizing the power consumption/dissipation in the design. This is used with hardware description languages likeVerilog, System-Verilog and VHDL. The major areas of concerns are simulation, emulation, static or formal verification, logical synthesis, DFT, placement and routing etc.

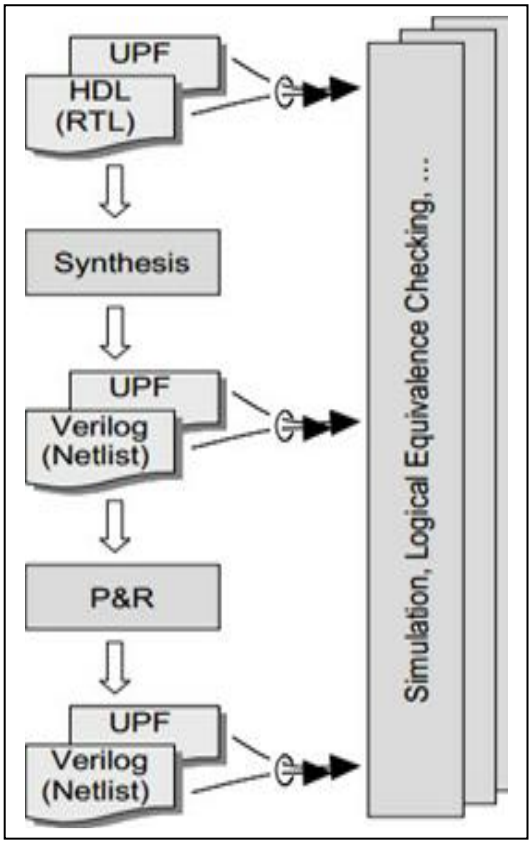
Keywords: Low Power, Synthesis, Unified Power Format, Accellera.

1. Introduction:

In the world of mobile apps, it's vital to attenuate power dissipation within the various chipset parts that aren't used. Now, chipsets contain various systems on the SoC. Every of these SoC is known as intellectual property (IP). That is why I want less power consumption, individual IP can locomotive in-between regular power modes i.e., power-off and power-on/sleep. Individual IPs is basically partitioned into various power-domains, and individual's power domain can be switched on/off as well, based on the mode of power. The contents of memories and registers are restored after being shut down in a feasible manner (commonly known as retention). There are isolation-cells that remain the outputs of power intent which are turned off in previously defined states, and in this way the shut-down power intent will not manipulate the functionality of power intent. Our power management verification practices enable us toverify the functionality of all segments that are narrated above formal ones is highly advisable. Such techniques should ensure that not only power intentions have been fully and properly implemented, but also the design carries its correct

operations even after the insertion of power management strategies. In industries commonly used power format design method in low power designs in Unified power format (UPF) it is designed to envision the power intent of the design at a comparatively high level.UPF (Unified-Power-Format) allows a design engineer to design electronic systems maintaining power as an essential contemplation in the early phases of the design process.

For example, specifications for the implementation of power information in the first steps of the Register-Transfer -Level (RTL) propose procedure. Fig 1 shows UPF inclusion in the design flow. The UPF provide a single configuration plan that is used to detail control sensitive intend in order thatpossibly will not be indicate in the Hardware Description Languages (HDL) alternatively if we can't declare it explicitly in the code, we can include the required material in the constrained power intended design by using UPF. UPF provided is same in both verification and implementation. That is what must be verified is implemented in UPF design.As shown in Fig 1, UPF files are combined with RTL (Register-Transfer-Logic), these UPF files relate to the power-intent of the designer. These UPF files relate to the power-intent of the designer. A variety of tools, such as simulation tools, synthesis tools and formal verification tools, use the assortment of source files included in the UPF as input data.



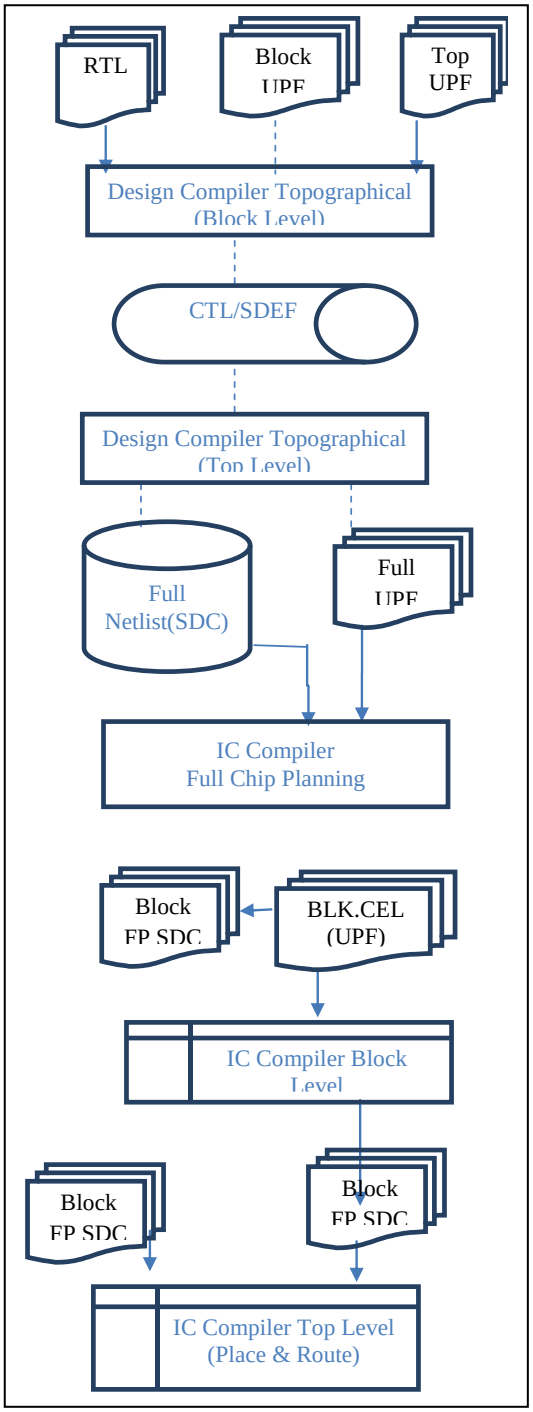


Fig. 1 UPF WorkflowFig. 2 Synopsys EDA tool based UPF design flow.

It is a capability for creating a concise intended design specification. The term "power-intent design" can be used to a wide range of design components. UPF specifications are stored with the other IP (intellectual property) block resources and re-used with the other resources of an IP (intellectual property) blocks and re-used along with the IP's other supplied files It facilitates automation in verification and implementation by carefully documented semi logy, pliability in specification, and, when necessary, described logical

limitations.The long-term goal of this technology is to provide a fully automated tool that catches changes in HDL code and updates the UPF accordingly (and vice-versa).

Fig. 2 Synopsys EDA tool based UPF design flow. This work is organized as flows: The first section contains an introduction. The second section summarizes the preceding work. The design process is covered in Section 3, and the findings and discussion are covered in Section 4.

2. Previous Work

R. Koster., et al. presents Low-power designs necessitate forceful power control and verification [1] and implementation problems are challenging. IEEE Standard 1801 Unified-Power-Format (UPF) allows for the first confine of control intents, untimely confirmation of power administration, and automatic execution of power intent in low-power systems. This paper presents a high-level overview of UPF concepts, commands, applications, and flows, for mutually IP blocks and system.To detect structural Low-power design issues, static verification can be performed at both the RTL and netlist level. Static verification is used to assess a design and ensure that its functionality is maintained. When the driving logic of a logic signal isn't active, an isolation approach is used to give it a defined behaviour. An isolation cell passes normal logic values throughout ordinary process and clamps its output to a specified logic value when a control signal is asserted. V. Gourisetty., et. al. [2] Explain the Low Power Design Flow utilising the UPF base low power design flow by means of Synopsys synthesis and physical implementation EDA tools within the Fig below. The flow starts with the design's Register-Transfer-Level (RTL) description and a discrete UPF interpretation of the design's power aim.The RTL and UPF interpretations are written in two separate files to allow for independent maintenance and editing. The compiler reads the RTL logic and original UPF power objective interpretations and generates a gate-level netlist and an updated UPF file (UPF') based on their contents. The UPF file contains the original UPF information as well as the precise supply net connections for specific cells created during the synthesis process.

3. Design Methodology

The main strategy is described here.

3.1 LibraryRequirements for Low Power Designs

There are numerous energy-saving strategies in use today. Power-gating, clock-gating, and multiple voltages are examples of technology libraries that must adhere to library syntax.

3.2 Level Shifter Cells

Whenever signals flow from any power domain with different voltage to another power domain in power intent design a level shifter should be used to avoid the corruption of a signal. In the Fig 3. With a single provide power at the input pin and a separate or higher voltage at the output pin, it acts as a buffer.

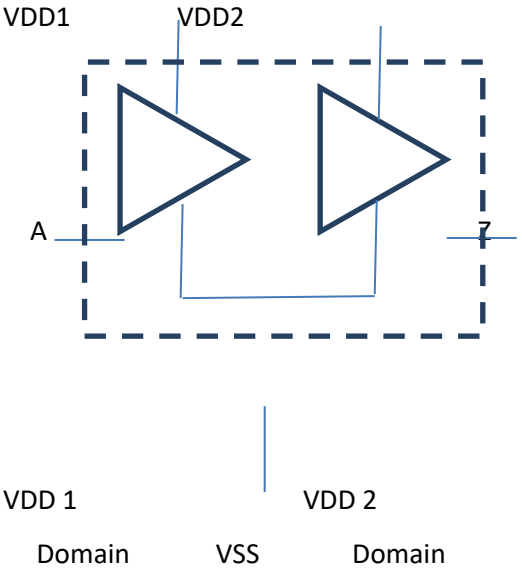


Fig. 3 Level Shifter

Thus, there is delay from input signal to output signal because the logic changes a signal crossing from one voltage level to required voltage. There are three types of level-shifter cells:

1. H2L level shifters (high voltage to low voltage) level shifters (low voltage to high voltage) level shifters (low voltage to high voltage)
2. L2H Level shifters (low voltage to high voltage) level shifters (low voltage to high voltage) level shifters (low voltage to high voltage) level shifters (low voltage (L2H)
3. Level shifter with the ability to convert H2L and L2H

The level shifter cell will include a library specification which provides description about the conversion performed like the voltage supported by shifter cell, is the conversion from logic 1 to logic 0, vice versa, or both and information related to the power pins that should be connected to individual power supply.

3.3 Isolation Cells

In Fig 3.2 a signal is crossing from the power domain which is powered down to which power domain that cannot be powered down, in such power-gating design, an isolation cell is required. This cell functions similar to buffer when both the input power-domain and output pin power-domain are powered on but provide required output when the input power domain is powered off.

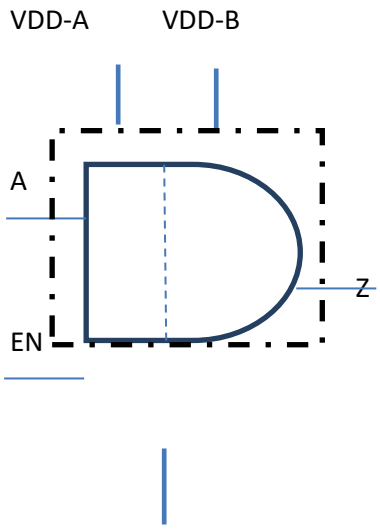


Fig. 4Isolation Cell

This cell functions similar to buffer when both the input power-domain and output pin power-domain are powered on but provide required output when the input power domain is powered off.

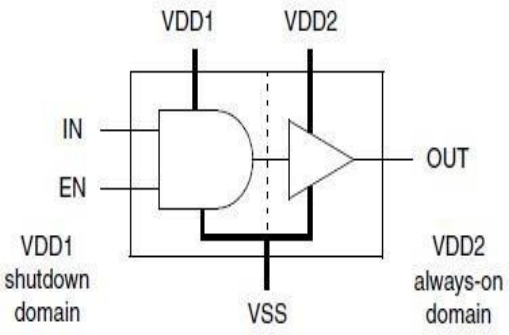


Fig. 5 Enable Level Shifter

3.4 Power Switch Cells

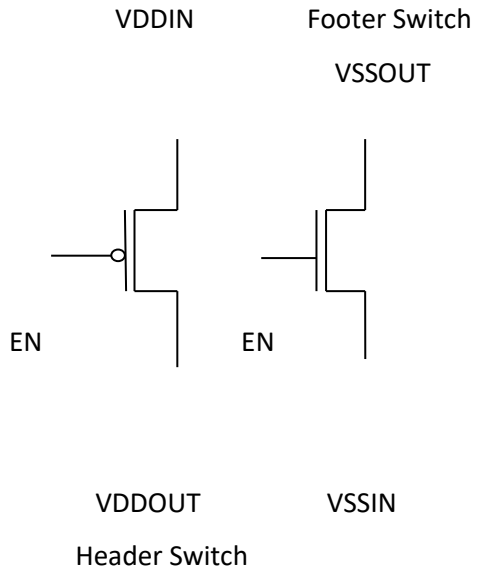


Fig. 6 Power Switch Cells

In header type power supplies, the power switch links the power supply pins to the power rail inthe designed power-domain. The ground rail is connected to the power source in the influence domain by a footer type power switch, as shown in Fig6, An input logic signal reins the association or separation status of the power toggle.To send power to cells that can be turned down in a low power management scheme that incorporates power gating, header or footer type power switch cells are required.

3.5 Always ON Logic Cells

As shown in Fig 7, when dealing with shutoff power-domains, there can be some conditions where specific cells in the shut-down portion must remain active indefinitely retention registers, isolation cells, retention control routes, and isolation enable paths all require this.

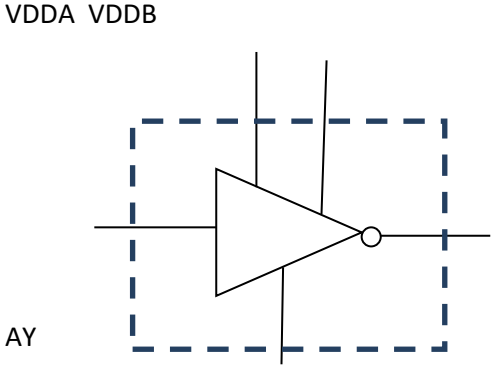


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Fig. 7 Always-On Logic Cells

Consider an example; an always-on buffer cell must be incorporated in the design when a signal crosses through a shut-down voltage area. Always-on logic, which is built with always on library cells, is the name for this type of logic. A functionally comparable always-on cell features a backup power supply that operate endlessly, even during the shut-down, as opposed to an ordinary cell.

3.6 Retention Register Cells

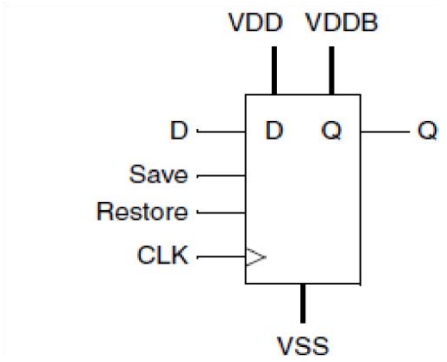

Fig.8 Retention Register Cells

Low power design contains power management strategies like power-gating. The designs in which power-gating is used there might be scenarios where we lose a data stored in registers.There are various methods to store the registers when powered down and restore it back when powered up.Retention registers are used to save and restore data back into the registers when the powered. As shown in Fig 8, it has a low-leakage network and a power source that is always turned on.

3.7 Power Domains

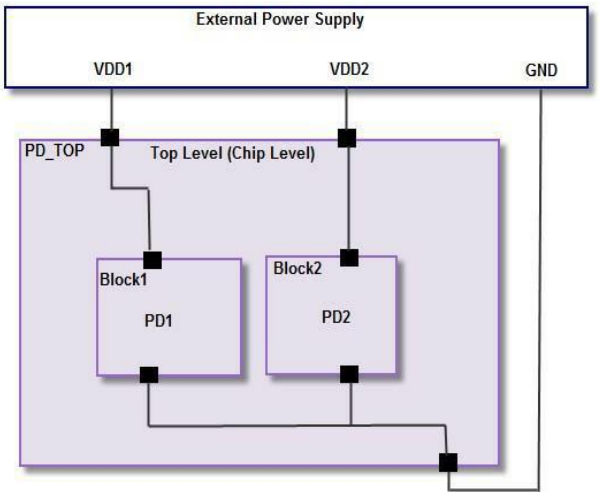

Fig.9 Power Domains

The “power-domain" is a set of design attributes that contribute to a standard power supply distribution network. Each strengthareaconsists of a scope and a quantity. The span is the hierarchical stage at which the area is described and is an ancestor of the strengtharea components, while the quantity is the realseries of strengtharea objects. In a strengtharea, simply one number onedeliverinternet is necessary.A “power-domain” has the following characteristics:

- Name
- Level of hierarchy or scope is required where the power domain is defined or created
- The power domain is made up of a collection of design elements.
- Associated group of supply nets that are allowed to be used inside power-domain Principle power supply and ground nets.
- Synthesis strategies for isolation, level shifters, always on cells, and retention registers.

In accumulation to the pinnacle-degreeelectricity domain, PD_TOP, there are extraelectricitydomain names defined, known as PD1 and PD2, created on thedegrees of hierarchical blocks, Block1 and Block2, respectively. Each block has deliver ports (proven as black squares with inside the diagram) to permitdeliver nets to go from the pinnacledegree down into the block degree.The following commands define the power domains of a design and assign hierarchical blocks to the domains:

construct power domain TOP create power domain PD1 – elements {A/D} create power domain PD2 – element {B/E/J} create power domain PD3 -elements {B/F} create power domain PD-elements {B/G}

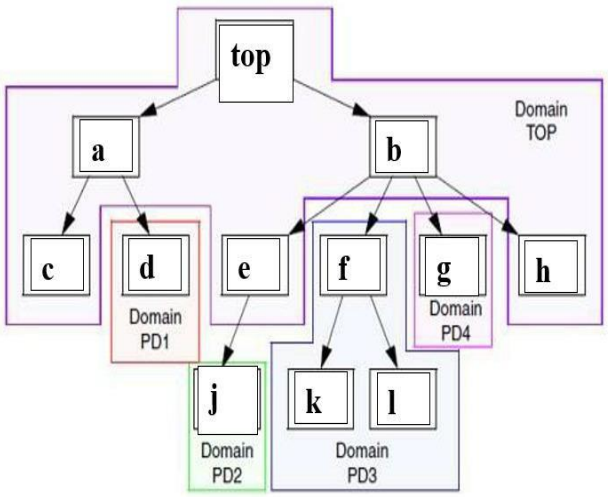

Fig.10 Power Domain Hierarchy

The pecking order and power domain partisanship of this example are illustrated in Fig 10.Power Distribution Elements:The following topics describe the power elements that allow you to specify the power intent of a design.

- Supply ports
- Supply nets
- Power Switch
- Supply Sets
- Supply Set Handles

4. Results and Discussion

4.1 UPF Clamp Value Debug System:

There are two modes in which an isolation cell can operate. Operation of isolation cell depends on isolation enable signal. The two modes of operations are Normal mode, acts as a buffer and isolation mode, which clamps the output to a specified value. The value of the clamp signal is critical in defining the isolation cell's definition

VDDA VDDB

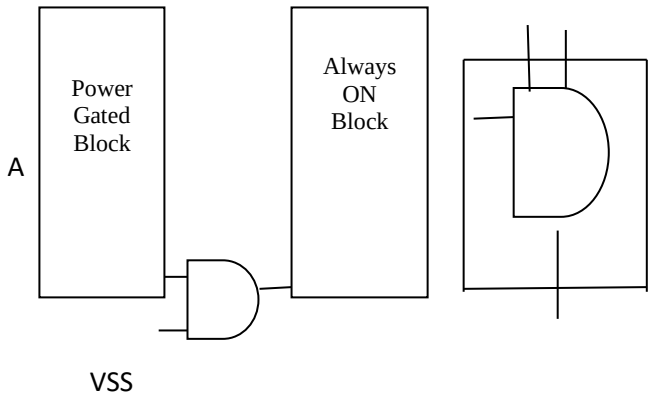

Fig. 11 Isolation Cell Placement

4.2 Wave Review of Wrong Clamp Value

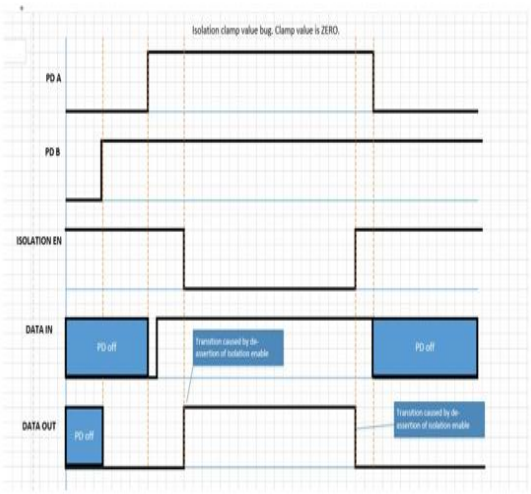

Fig12.Waveforms of clamp values

There Wrong clamp value can cause design bugs, for example: risk of glitches due to sampling of asynchronous signal leading to meta-stability posing both circuit and logic risks, a risk might not be caught in static simulation (i.e., spyglass) nor dynamic simulation (i.e. VCS). The propose an innovative strict method to eliminate this validation hole. The complexity of today's SoC design continues to grow with low-power devices. Nowadays, SoCs introduce many UPF (Unified Power Format) isolation strategies.

These strategies apply to a very large number of signals. In currently applied validation methodologies, there is no tool, dedicated to validating the correctness of clamp value specified in the UPF isolation strategy.

4.3 Asynchronous glitches

This is a new innovative approach aimed to validate and manage asynchronous glitches caused by wrong

UPFs clamp value. It may discover bugs in early stages, and therefore promote affective shift left in schedule. The current dynamic and static validation approaches do not aim nor capable to catch those asynchronous glitches. The solution suggested here is a system capable of finding violations caused due to wrong clamp value alongside with managing large amount of violations and waivers in a huge design such as client SoC (ICL client introduced ~15K violations). The proposed solution can be deployed in different IPs (sub systems) as well. It can shift left a project / Step by saving valuable time, violations can be found in IP or integration level as it allows user to run this check ahead of time rather than run last minute paranoia mode.

4.4 Checker of Clamp Violation

Bind checker is defined and enabled using the knob, (BIND_ISO_CHECKER_EN=1). It should contain module, elements, parameters, and ports as well as the signal paths which will be used for the checker. Its very important to check this parameter which clearly shows if any violation exits in the design module.

```
set CLAMP $iso_detail(clamp_value)
if {$CLAMP == "one"} {
set CLAMP_VALUE [list CLAMP_VALUE 1]
}
if {$CLAMP == "zero"} {
set CLAMP_VALUE [list CLAMP_VALUE 0]
}
set ISO_PWR_NET_NAME [list ISO_PWR_NET_NAME $iso_detail(isolation_power_net)]
set ISO_GRND_NET_NAME [list ISO_GRND_NET_NAME $iso_detail(isolation_ground_net
set ISO_IN_GEN [list ISO_IN_GEN UPF_GENERIC_DATA]
set ISO_OUT_GEN [list ISO_OUT_GEN UPF_GENERIC_OUTPUT]
set ISO_FULLNAME @$PD.isolation.$ISO_POLICY
set ISOPOLICY1 [list ISOPOLICY1 [query_original_name $ISO_FULLNAME]]

set ports_list {}
lappend ports_list $isoGround $isoSupply $ISO_IN $ISO_OUT $ISOEN $PD_SIMSTATE
set params_list {}
lappend params_list $PD_NAME $ISO_PWR_NET_NAME $ISO_GRND_NET_NAME $ISOPOLICY1
#puts $ports_list
#puts $params_list
if { [regexp {\S+} $iso_detail(isolation_power_net) ] ==1 } {
    if { [regexp {\S+} $iso_detail(isolation_ground_net) ] ==1 } {
        if { [regexp {\S+} $iso_detail(isolation_signal) ] ==1 } {
bind_checker no_iso_msg \
-module iso_checker \
-elements @$PD.isolation.$ISO_POLICY \
-parameters $params_list \
-ports $ports_list
}
}
```

Fig13.Syntax of Bind_checker

5. Conclusion

In this paper, the main part was to work on developing the checker, the bucketing of violations and validate with help of each IP owners. The script is developed such that it is used to generate clamp valuation report, segregate the variations with updated waiver files. The script helps to segregate the violations with respect to

the IP owners TI and report them. The respective IP owners validate each signal with Verdi tool and report which are real Bugs, fixes and rest are waived. There would be more than 9000 clamp violations which may contain different bugs, fixes required that is got from the clamp violation checker. For every new release model, test has run and generated the report. Finding the new violations with respective to different IP and examining between the tests results of previous and current reports. It is considered as the paranoia checks on the SoC.

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