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Image Processing And Applications On Hardware And Cryptography

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Abstract:

The increasing importance of embedded applications in various domains such as image processing, video processing, and communication has raised the concerns of researchers Computer vision is a domain where hardware implementations outperform software. In this field, we have seen that the development of very powerful hardware devices such as FPGAs has allowed embedded designers to create truly unique designs. Communication of video and image data in multiple FPGAs is no longer an isolated issue. This paper shows how to develop hardware-based computer vision algorithms that can be used to transmit and receive video and image data from multiple FPGAs.

Keywords ASIC,DSP image thresholding, Security ,RC4, Image processing, Field Programmable Gate Array (FPGA)

Introduction

Human perception and intelligence are the key factors that make vision processing fascinating to the research community. It can be used to augment the capabilities of machines such as video surveillance systems and robotic assistants.

Video processing hardware designs are typically built to address the needs of the end users while keeping security and performance concerns in mind. Before the initial processing step is carried out, various predefined steps are performed to enhance the original image quality. The next step involves separating the objects from the background and performing feature extraction.We introduce image thresholding as a technique that enables the pre- and segmentation stages to be performed in a way that is optimized for the best possible performance.

Existing Methods:

1.Segmentationon image thres holding:

Binarization is the process of extracting binary image from various sources. In this stage, the image should contain no more than two-pixel values. Binarization is very common in image processing and analysis.

To extract the most useful information from an image, its components must be separated into two parts, the foreground, and the background. The former is where the gray level pixels are located, while the latter is where the red level pixels are located. A thresholding technique is used to separate the objects from the background.Due to its simplicity and its efficiency, thresholding has been studied extensively. Numerous thresholding techniques have been published in the literature.

A dedicated FPGA hardware can process image in real time, while consuming less power and making it easier to use. An FPGA application can run at a speed of up to 2x faster than the same software component.A thresholding algorithm is a technique that can be used to reduce the image's pixel intensities. It is typically performed as a function of the image's pixel intensities and thresholding is a process that involves finding the ideal value for an image. This step can be performed by analyzing the image's dominant factor at the end.

b(x) =1ifh≤a(x)≤ k

0 otherwise

In image processing, where x is the form x1, ith coordinate is a real number that denotes the sum of the digits of x. Most commonly, ith coordinate is used to denote the subsets of n-dimensional space Rn. For Otsu's method, the data must be sent to the luma component Y to get the grayscale image intensity data. In our model, the data is treated as their greyscale equivalences, which means that it saves a lot of time and effort. In this paper, we introduce a clustering-based method to calculate the threshold for various types of image problems, which are mainly presented as degraded documents, aerial images, texture, normal colour images etc. Our method achieves good results in terms of recognizing normal and degraded images.

$$a=\sum_{i}^{m} \sum_{j}^{n} \frac{p(i,j)}{m\,x\,n} \quad (1)$$

Where m n is the grid dimension, the pixel coordinates are i and j. If the grid dimension is not specified, then the pixel coordinates are not consecutive. The authors had proposed an optimized threshold architecture for medical imaging applications. However, it was not ideal for dynamic thresholding due to its selection being static. This paper proposes an alternative approach which is based on behavioral simulation.

2: Multiple FPGA platforms on image data in secured transmission

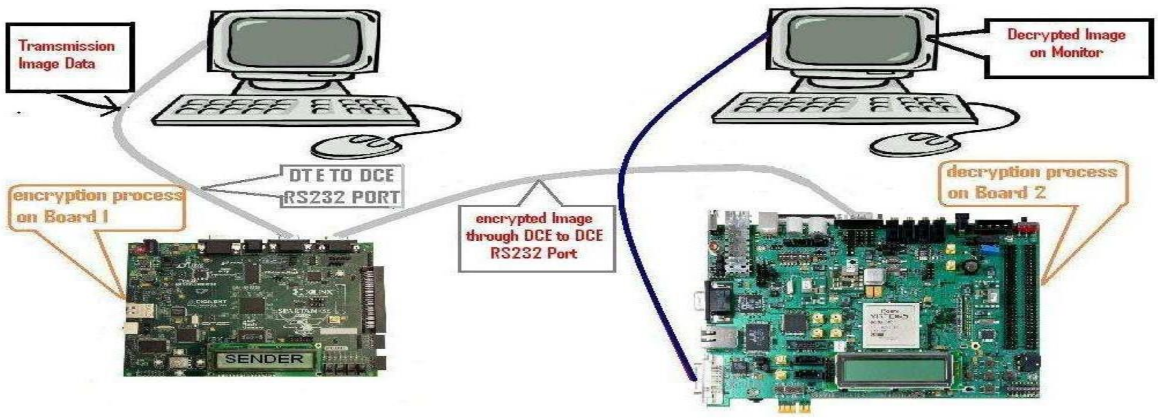


Fig1: FPGA platform

Due to the nature of the image applications, they are used in, they are not secure and could allow unauthorized users to access them. This work describes a secure hardware architecture that serves as the main component of an image transmission.

3. Hardware architecture and implementation design:

Fig. 1 shows the architecture of multiple FPGA platforms that communicate with encrypted image data.Theimage filteringequation witha particularkernel isasshown as below

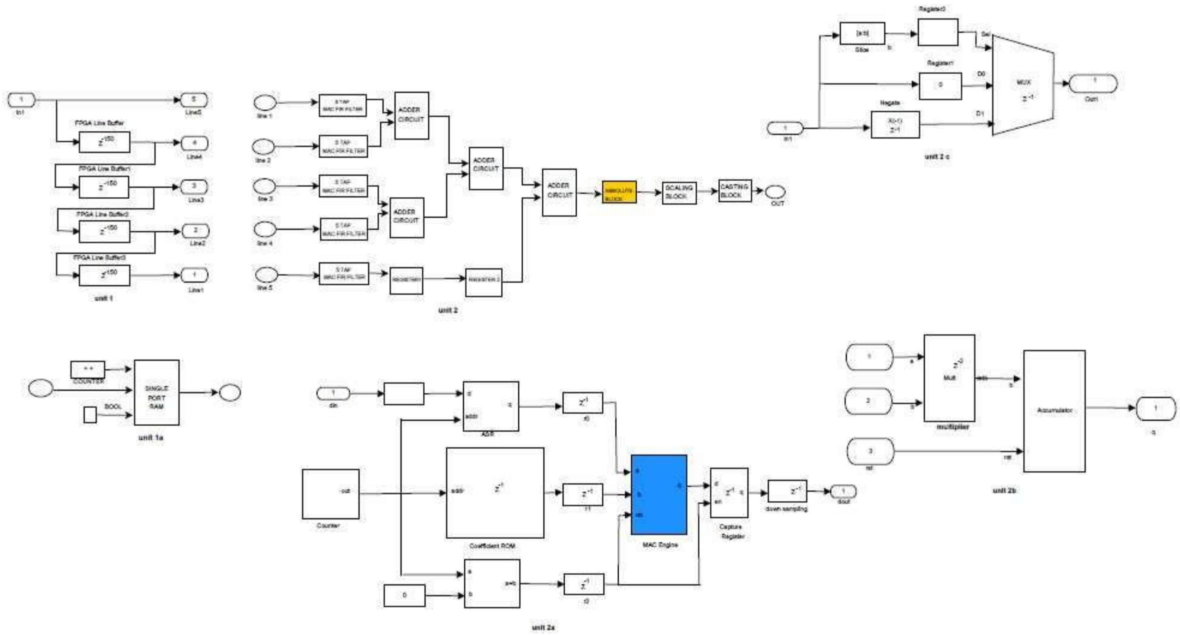


Fig2: Filtering hardware architecture

The image filter hardware consists of five buffer lines. The lines are selected according to the size of the filter's kernel. The output of each of the five buffers of unit-1 goes to the inputs of unit-2. The resulting output is computed by adding five MAC engines to the input. The blue block is the MAC engine of unit-2b. The yellow box is the absolute value of the calculation.

For Image thres holding asasegmentation step:

In cases of mixed media, such as colored images, it is broken down into 3 separate matrix structure channels, which are Red, Green, and Blue. Each picture is then processed in hardware for smoothing. The threshold for each color is computed separately for binarization and calculation.

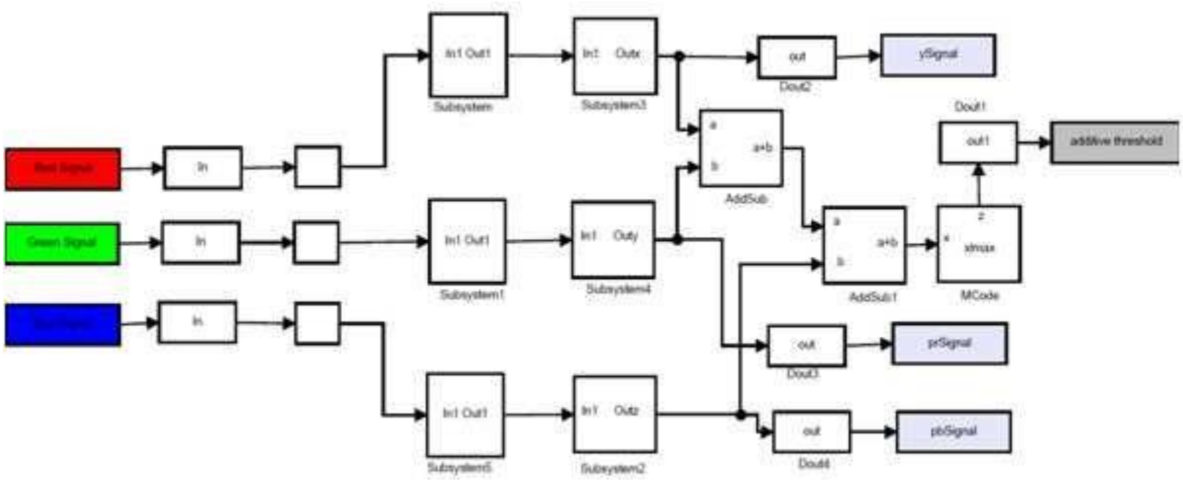


Fig3: Hardwarearchitecture

Steps to be Followed:

- Divide the colour image into its constituent components Red, Green, and Blue. For each channel, perform the following steps.
- Repeat for 1 to n to get the total number of occurrences in pixel intensity.
- For red, green, and blue matrices, divide the no of pixels present in each matrix into 3.

4. Results and Observation

For image thres holding:

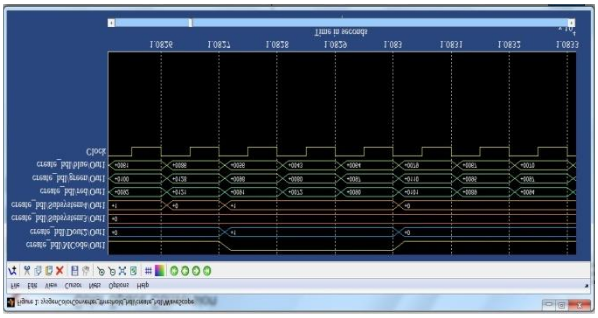
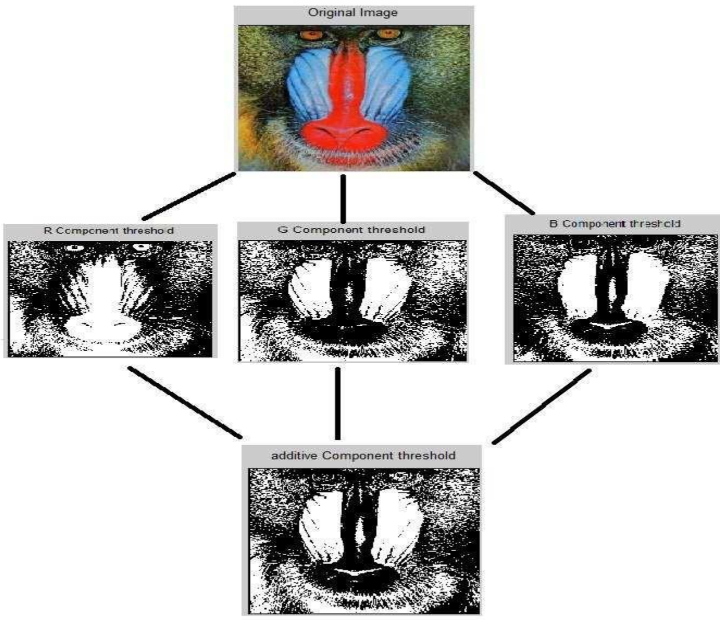


Fig 4: ISIM Viewer

The Wave Scope tool is a powerful tool that can be used to evaluate and debugging System Generator signals. It provides a graphical representation of the time-changing values of the wires in the design. The section displaying the parameter list and the results corresponding to it is divided into two. The



former has the values in decimal and the latter has the results in RGB.

Fig5: Binarization technique

Fig5.a

Fig5.b: Degraded documents

Each colored image is broken down into three sub parts namely, R, G, and B. These components are then added up to create the final binarised image.

5. Conclusion

This work mainly focused on the image processing domain and its implementation on various hardware devices. It also talked about the various steps that have been taken in this field and its potential applications. In the next few years, we could come up with some innovative ideas related to image security.

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